- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range . . . 0 V to 4.5 V (Min) with 5-V Single Supply**
- **No Phase Inversion**
- **Low Noise . . . 18 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C (TLV243xA)
- **Low Input Bias Current . . . 1 pA Typ**
- **Very Low Supply Current . . . 125 μA Per Channel Max**
- **600-Ω Output Drive**
- **Macromodel Included**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV243x and TLV243xA are low-voltage operational amplifier from Texas Instruments. The common-mode input voltage range for each device is extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. The TLV243x only requires 100 μA (typ) of supply current per channel, making it ideal for battery-powered applications. The TLV243x also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecom applications.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

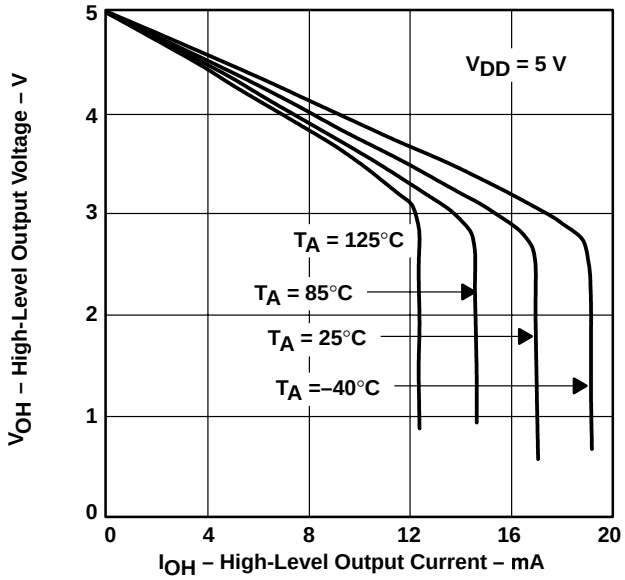

Figure 1

The other members in the TLV243x family are the high-power, TLV244x, and micro-power, TLV2422, versions.

The TLV243x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV243xA is available and has a maximum input offset voltage of 950 μV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TLV2432 and TLV2432A AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	2.5 mV	TLV2432CD	—	—	TLV2432CPW	—
–40°C to 85°C	950 µV 2.5 mV	TLV2432AID TLV2432ID	— —	— —	TLV2432AIPW —	— —
–40°C to 125°C	950 µV 2.5 mV	TLV2432AQD TLV2432QD	— —	— —	— —	— —
–55°C to 125°C	950 µV 2.5 mV	— —	TLV2432AMFK TLV2432MFK	TLV2432AMJG TLV2432MJG	— —	TLV2432AMU TLV2432MU

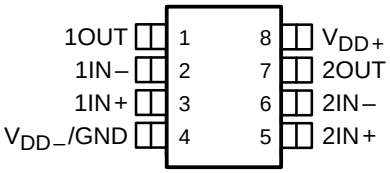
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2432CDR). The PW package is available only left-end taped and reeled.

TLV2434 AVAILABLE OPTIONS

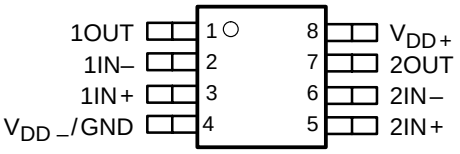
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
0°C to 70°C	2.5 mV	TLV2434CD	TLV2434CPW
–40°C to 125°C	950 µV 2.5 mV	TLV2434AID TLV2434ID	TLV2434AIPW TLV2434IPW

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2434CDR). The PW package is available only left-end taped and reeled.

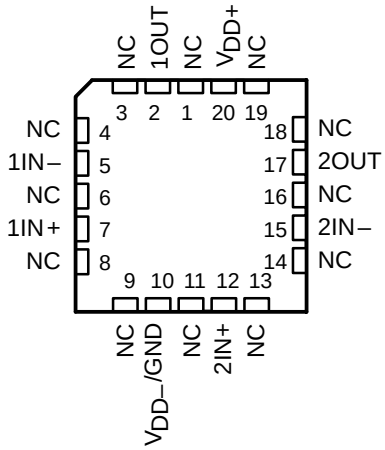
TLV2432
D OR JG PACKAGE
(TOP VIEW)



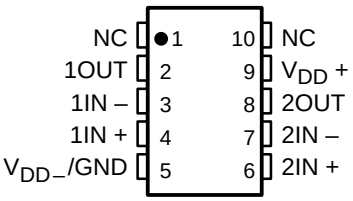
TLV2432
PW PACKAGE
(TOP VIEW)



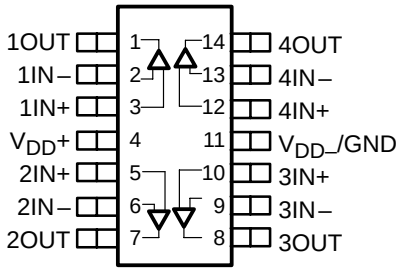
TLV2432
FK PACKAGE
(TOP VIEW)



TLV2432
U PACKAGE
(TOP VIEW)

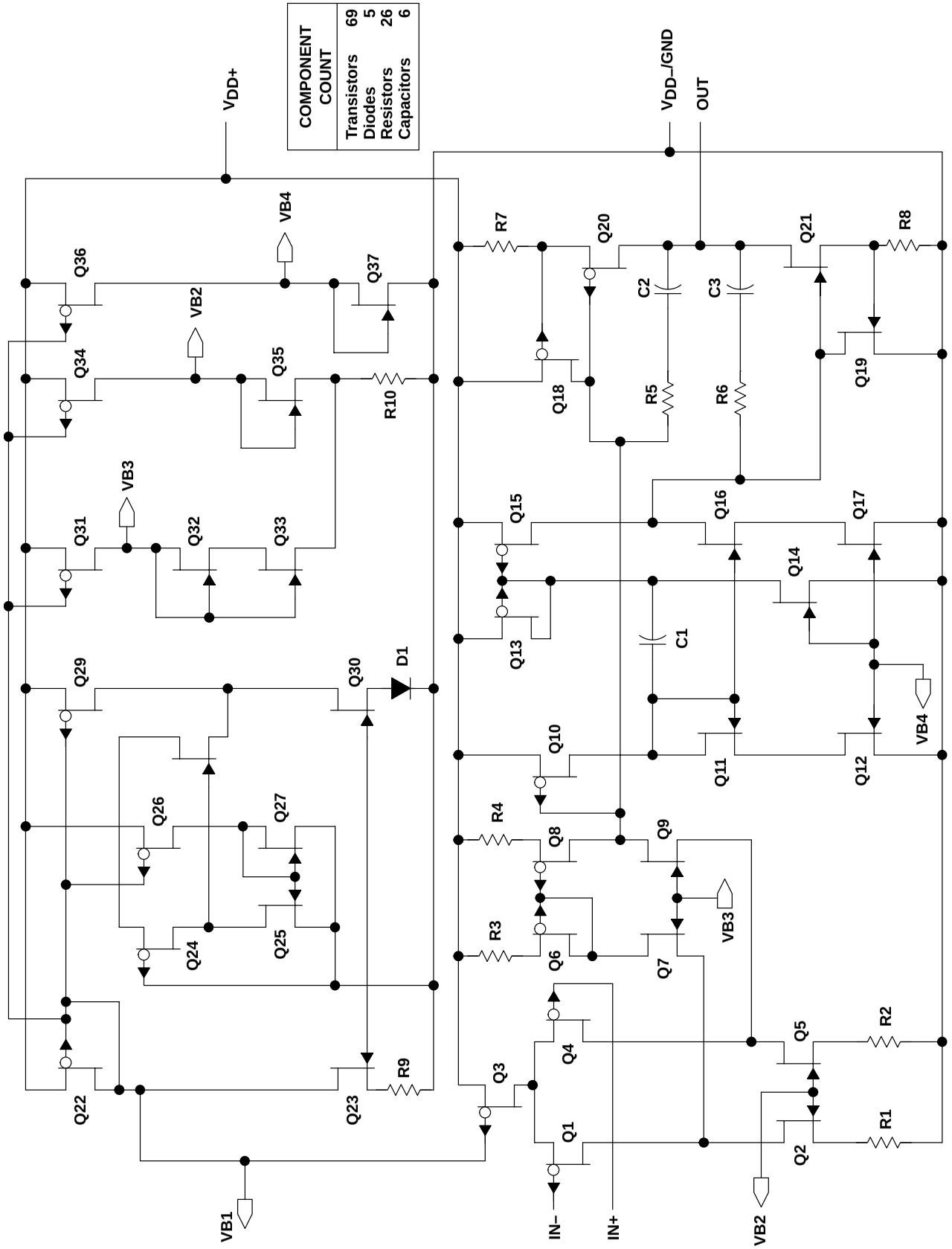


TLV2434
D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage, V_I (any input, see Note 1): C and I suffix . . . . . –0.3 V to V_{DD}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix (dual) . . . . . –40°C to 85°C
I suffix (quad) . . . . . –40°C to 125°C
Q suffix . . . . . –40°C to 125°C
M suffix . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14)	1022 mW	7.6 mW/°C	900 mW	777 mW	450 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW (8)	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW (14)	720 mW	5.6 mW/°C	634 mW	547 mW	317 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV243x			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, $V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	TLV243xC, TLV243xI	25°C		300	2000	μV
				Full range			2500	
			TLV243xAI	25°C		300	950	
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.5	–0.25 to 2.75		V
				Full range	0 to 2.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		2.98		V
		I_{OH} = –3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 100 μA	25°C		0.02		V
		V_{IC} = 1.5 V,	I_{OL} = 3 mA	25°C		0.83		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ‡	25°C	1.5	2.5		V/mV
				Full range	1			
			R_L = 1 MΩ‡	25°C		750		
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
$r_{i(c)}$	Common-mode input resistance			25°C		1000		GΩ
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		98	125	μA
				Full range			125	

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is – 40°C to 85°C. Full range for the quad I suffix is – 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV243x			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 2 V, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C	0.15	0.25		V/μs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120		nV/√Hz
		f = 1 kHz		25°C		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		μV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		0.065%		
			A_V = 10			0.5%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C		0.5		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 2 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		220		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		μs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡,	C_L = 100 pF‡	25°C		62°		
	Gain margin			25°C		11		dB

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is – 40°C to 85°C. Full range for the quad I suffix is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV243xQ, TLV243xM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, $V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	TLV243xQ, TLV243xM	25°C		300	2000	μV
				Full range			2500	
			TLV243xAQ, TLV243xAM	25°C		300	950	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.5	–0.25 to 2.75		V
				Full range	0 to 2.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		2.98		V
		I_{OH} = –3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 100 μA	25°C		0.02		V
		V_{IC} = 1.5 V,	I_{OL} = 3 mA	25°C		0.83		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ‡	25°C	1.5	2.5		V/mV
				Full range	0.5			
			R_L = 1 MΩ‡	25°C		750		
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
$r_{i(c)}$	Common-mode input resistance			25°C		1000		GΩ
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		195	250	μA
				Full range			260	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV243xQ, TLV243xM, TLV243xAQ, TLV243xAM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 2 V, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C	0.15	0.25		V/μs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120		nV/√Hz
		f = 1 kHz		25°C		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		μV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		0.065%		
			A_V = 10			0.5%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C		0.5		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 2 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		220		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		μs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡,	C_L = 100 pF‡	25°C		62°		
	Gain margin			25°C		11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV243x			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, $V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	TLV243x	25°C		300	2000	μV
				Full range			2500	
			TLV243xA	25°C		300	950	
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 μA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 2 kΩ‡	25°C	2.5	3.8		V/mV
				Full range	1.5			
			R_L = 1 MΩ‡	25°C		950		
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
$r_{i(c)}$	Common-mode input resistance			25°C		1000		GΩ
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load	25°C		100	125	μA
				Full range			125	

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is – 40°C to 85°C. Full range for the quad I suffix is – 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV243x			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C	0.15	0.25		V/μs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		μV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		0.045%		
			A_V = 10			0.4%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L =2 kΩ‡,	25°C		0.55		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 2 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		100		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		μs
			To 0.01%			13.1		
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡,	C_L = 100 pF‡	25°C		66°		
	Gain margin			25°C		11		dB

† Full range for the C suffix is 0°C to 70°C. Full range for the dual I suffix is – 40°C to 85°C. Full range for the quad I suffix is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV243xQ, TLV243xM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, $V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	TLV2453x	25°C		300	2000	μV
				Full range			2500	
			TLV2453xA	25°C		300	950	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 μA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 2 kΩ‡	25°C	2.5	3.8		V/mV
				Full range	0.5			
			R_L = 1 MΩ‡	25°C		950		
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
$r_{i(c)}$	Common-mode input resistance			25°C		1000		GΩ
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		200	250	μA
				Full range			270	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV243xQ, TLV243xM, TLV243xAQ, TLV243xAM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C	0.15	0.25		V/μs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		μV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		0.045%		
			A_V = 10			0.4%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L =2 kΩ‡,	25°C		0.55		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 2 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		100		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		μs
			To 0.01%			13.1		
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡,	C_L = 100 pF‡	25°C		66°		
	Gain margin			25°C		11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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V_O	Voltage-follower large-signal pulse response		35,36
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THD + N	Total harmonic distortion plus noise	vs Frequency	44,45
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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2432
INPUT OFFSET VOLTAGE**

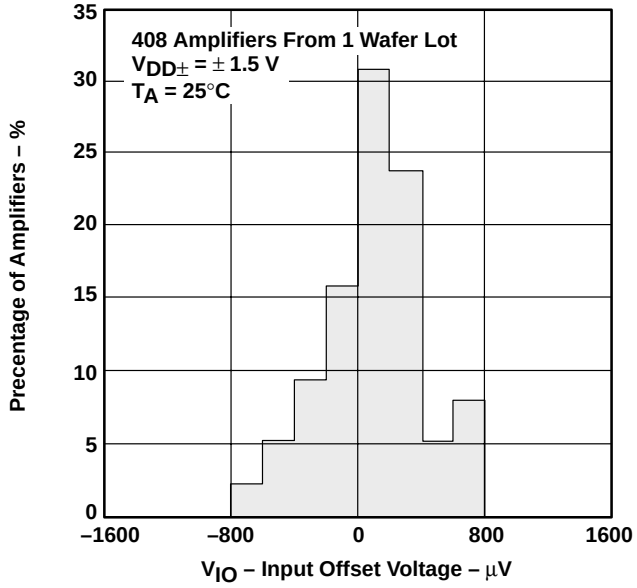


Figure 2

**DISTRIBUTION OF TLV2432
INPUT OFFSET VOLTAGE**

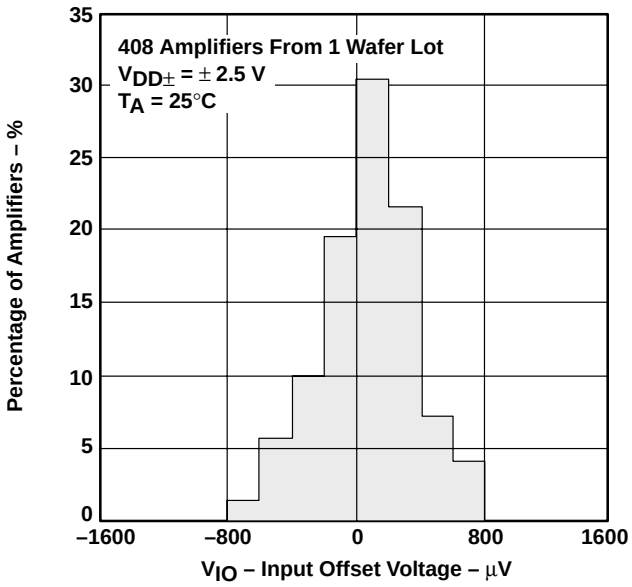


Figure 3

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

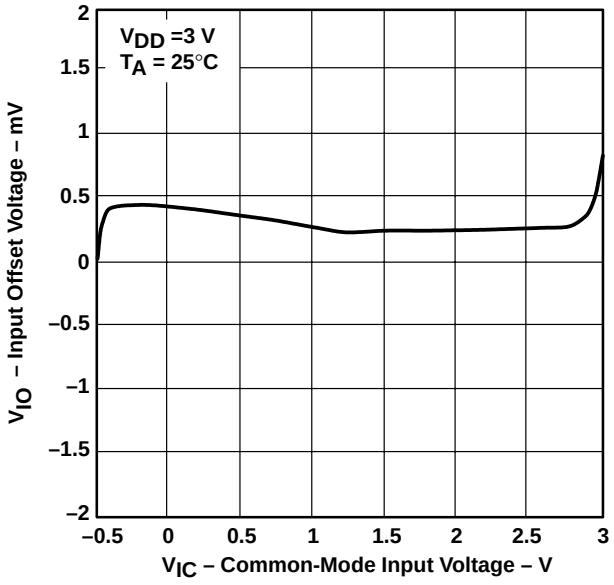


Figure 4

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

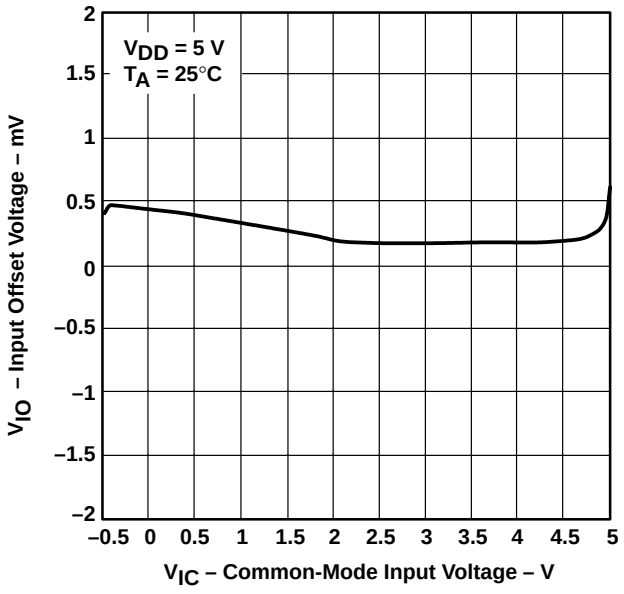


Figure 5

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2432 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

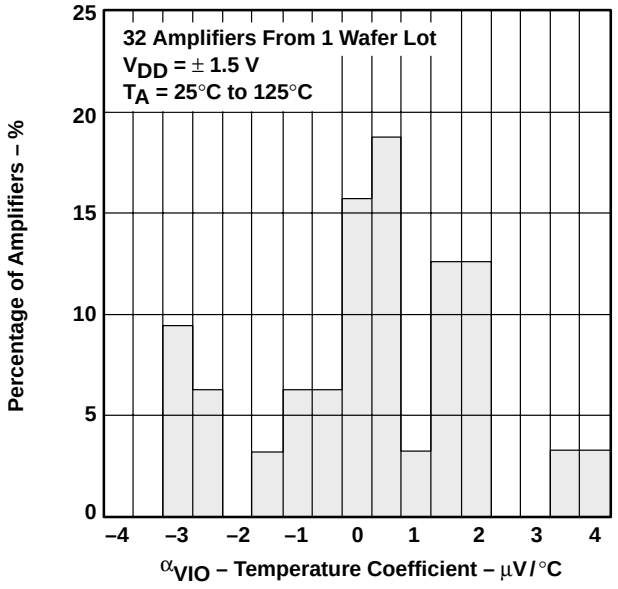


Figure 6

DISTRIBUTION OF TLV2432 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

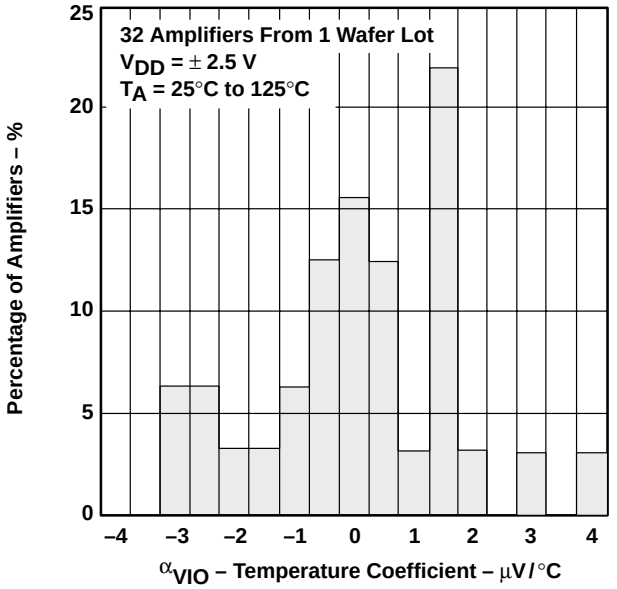


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

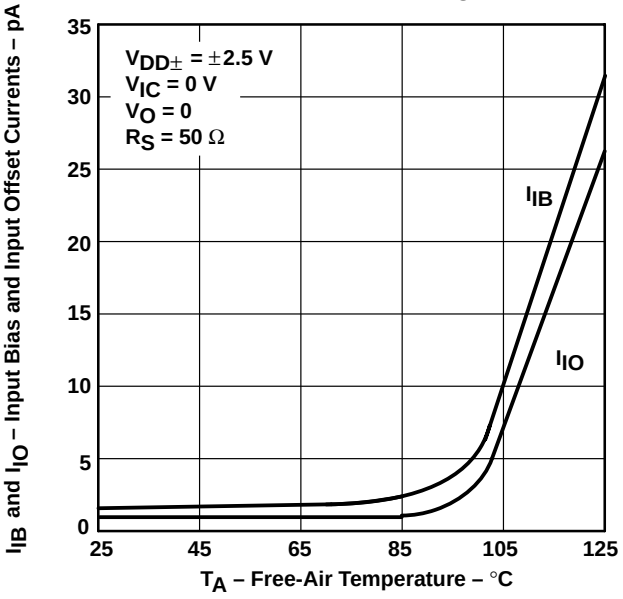


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

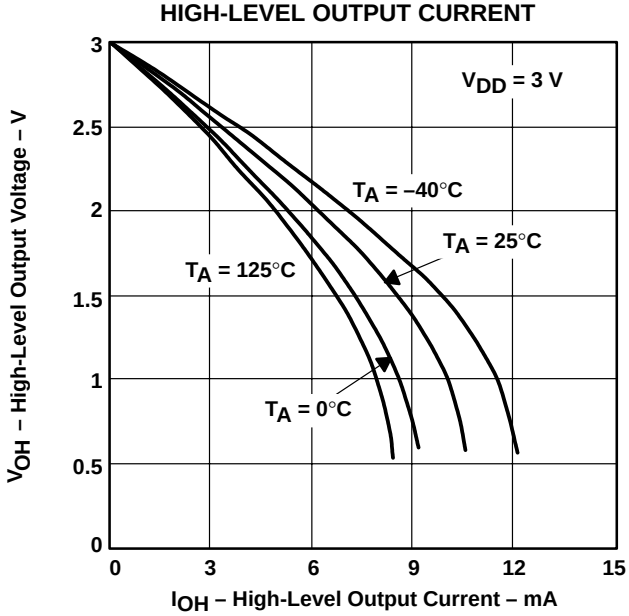


Figure 9

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

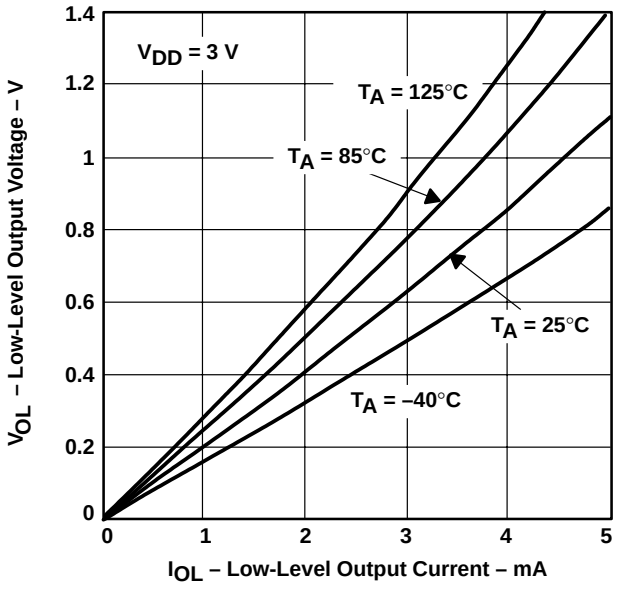


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

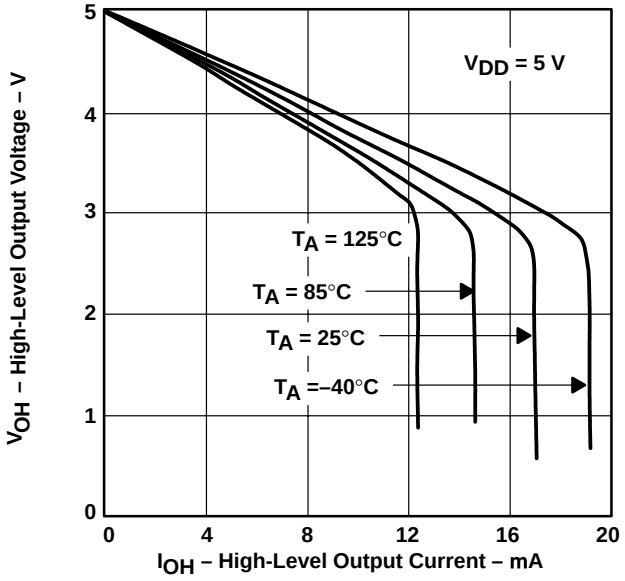


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

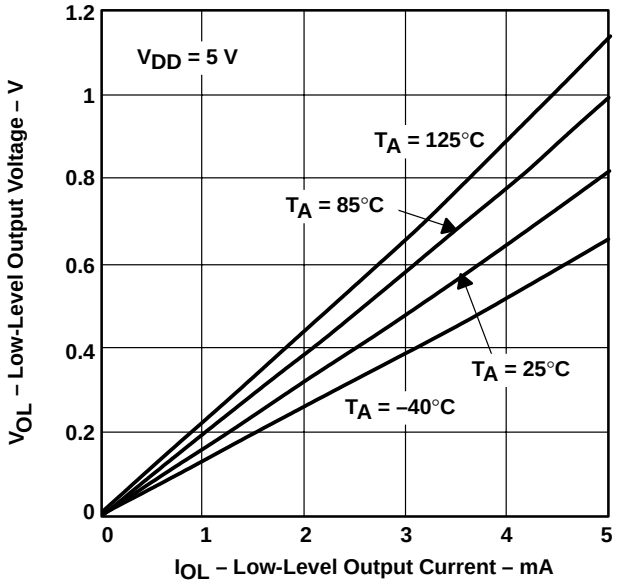


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

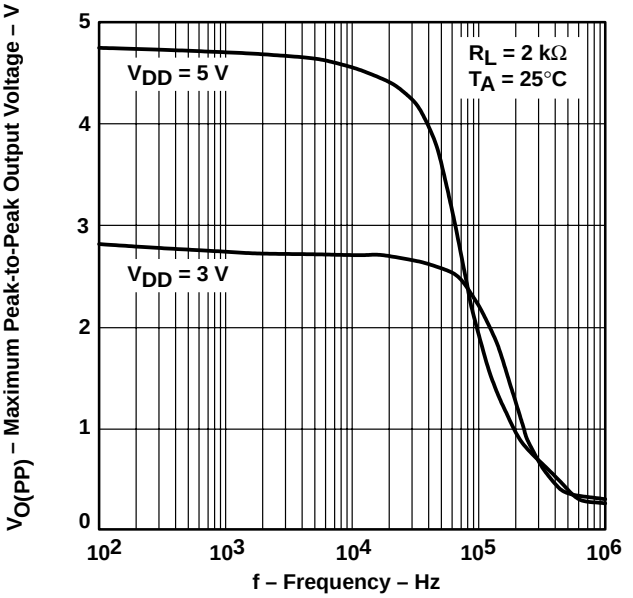


Figure 13

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

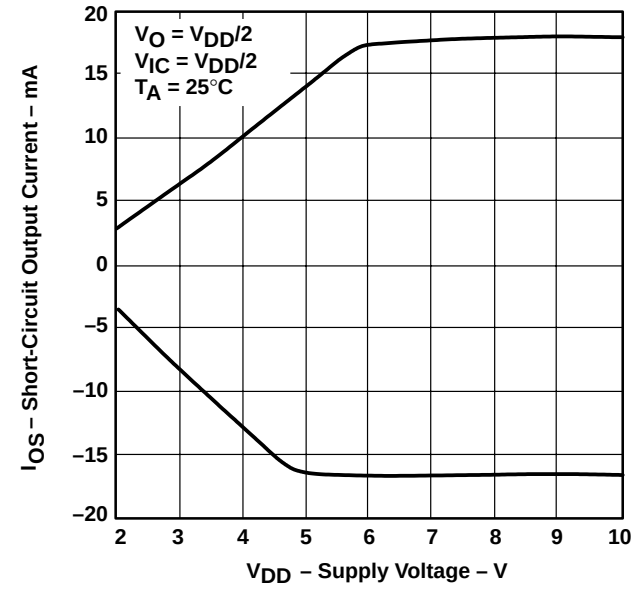


Figure 14

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

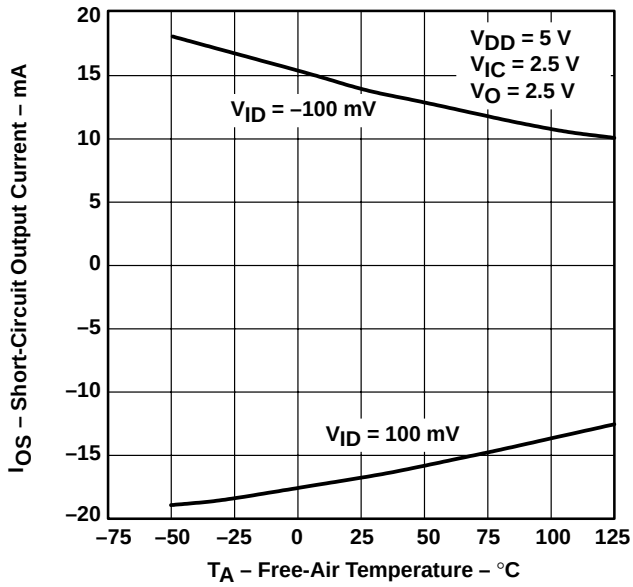


Figure 15

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

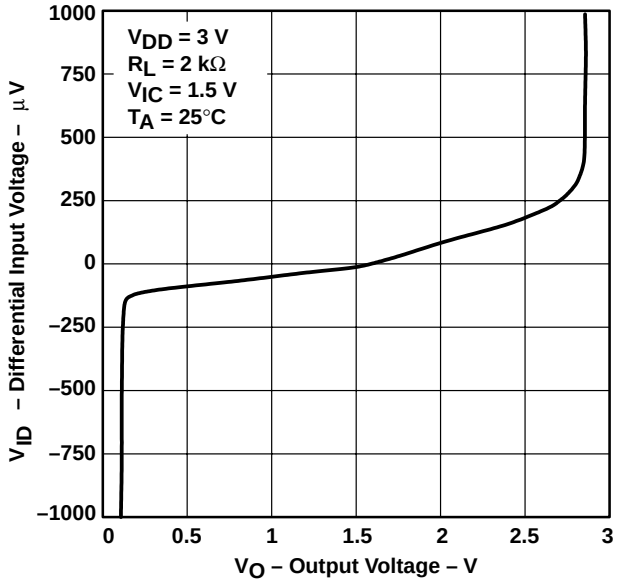


Figure 16

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

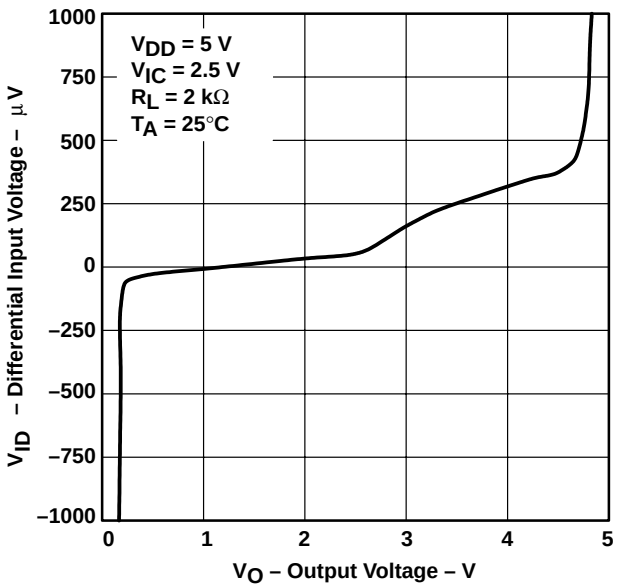


Figure 17

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN vs LOAD RESISTANCE

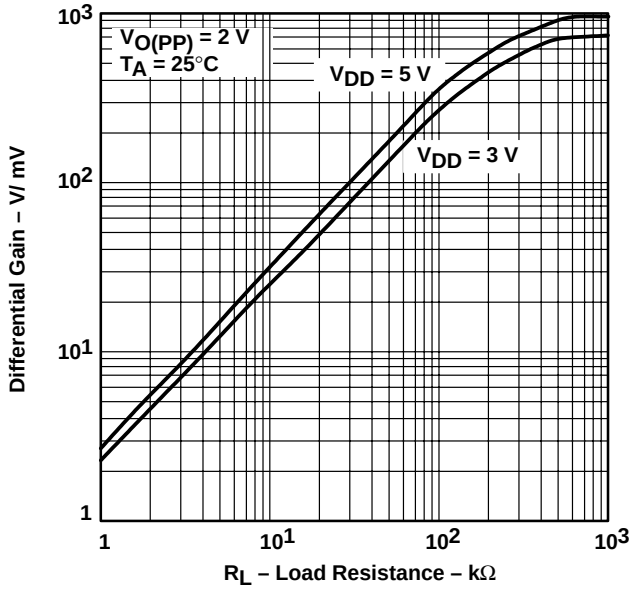


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

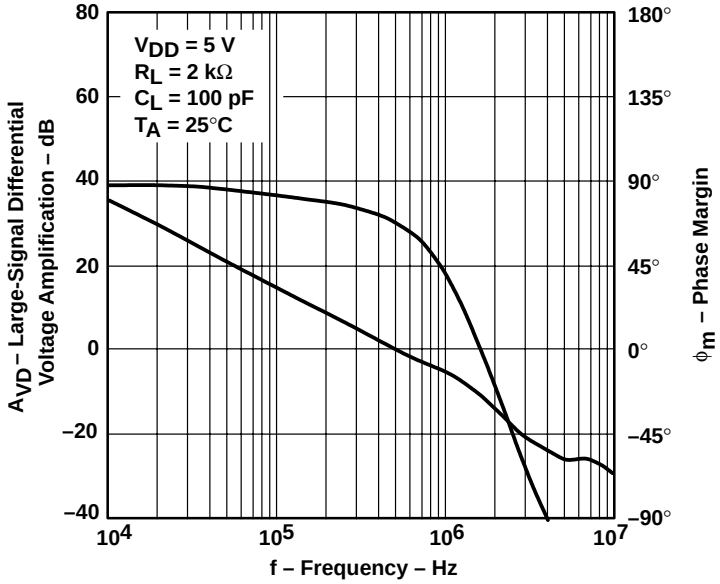


Figure 19

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

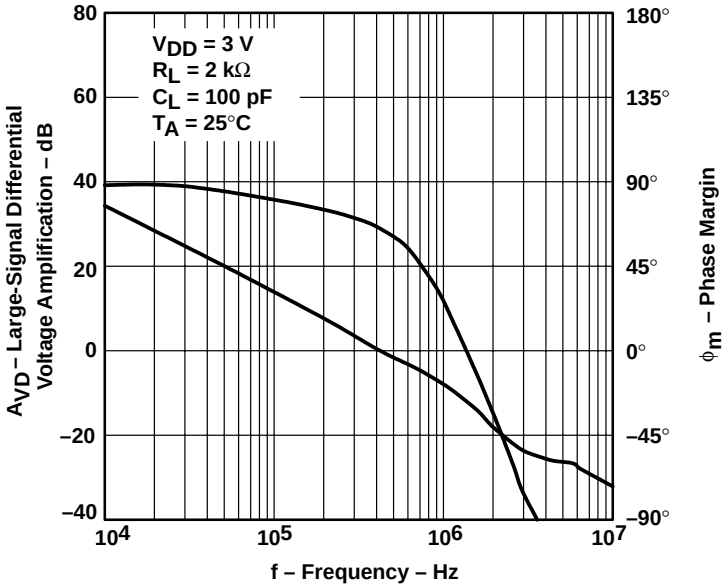


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

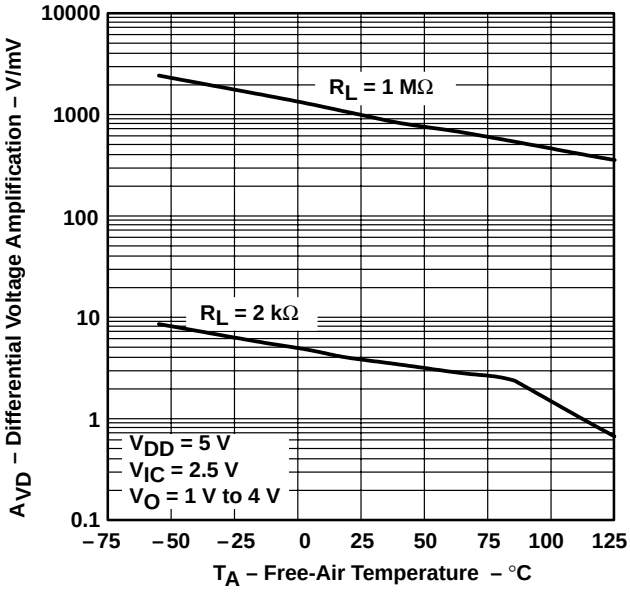


Figure 21

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

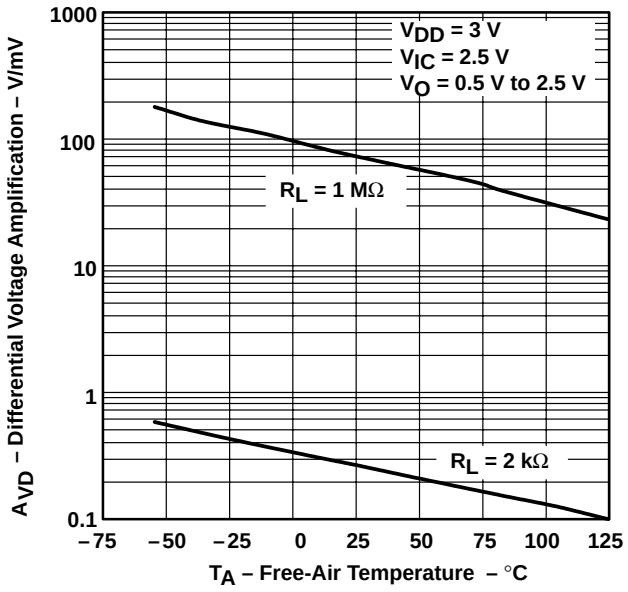


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

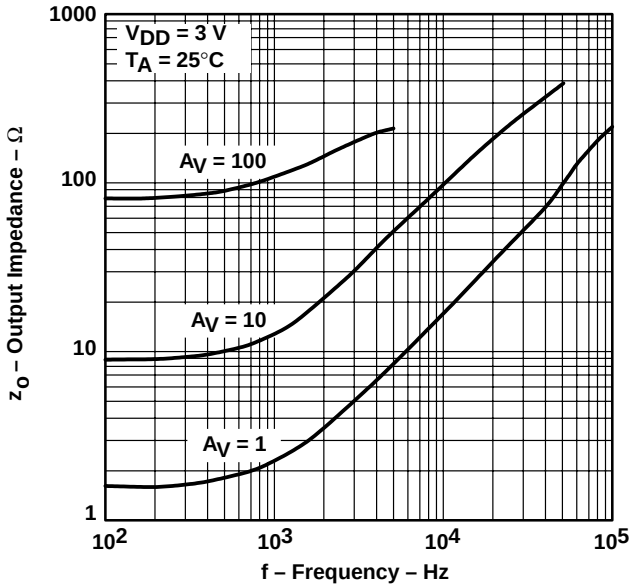


Figure 23

OUTPUT IMPEDANCE vs FREQUENCY

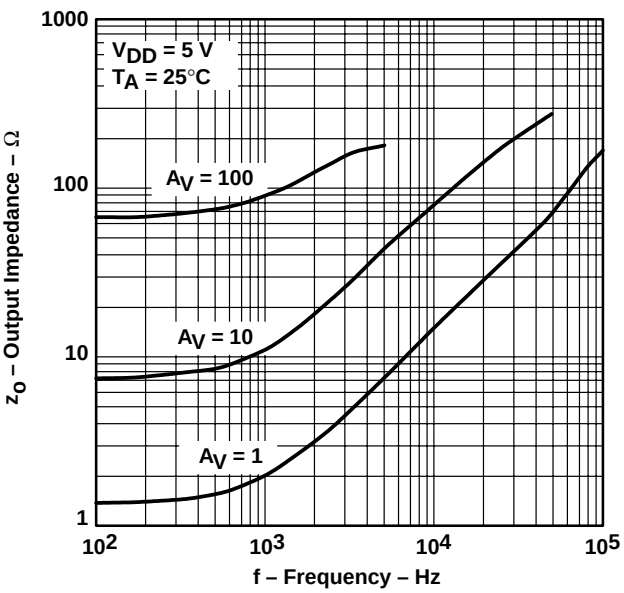


Figure 24

COMMON-MODE REJECTION RATIO vs FREQUENCY

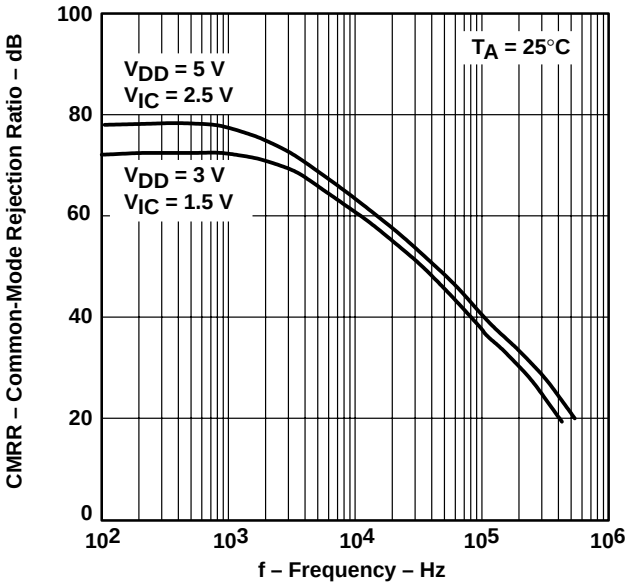


Figure 25

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

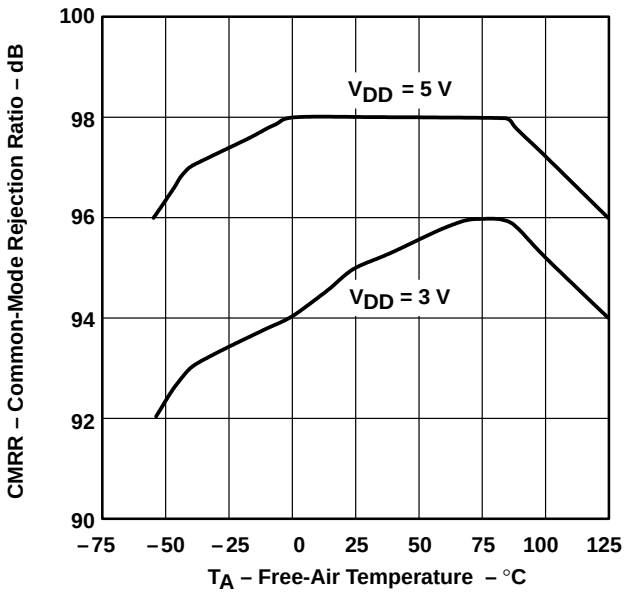


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

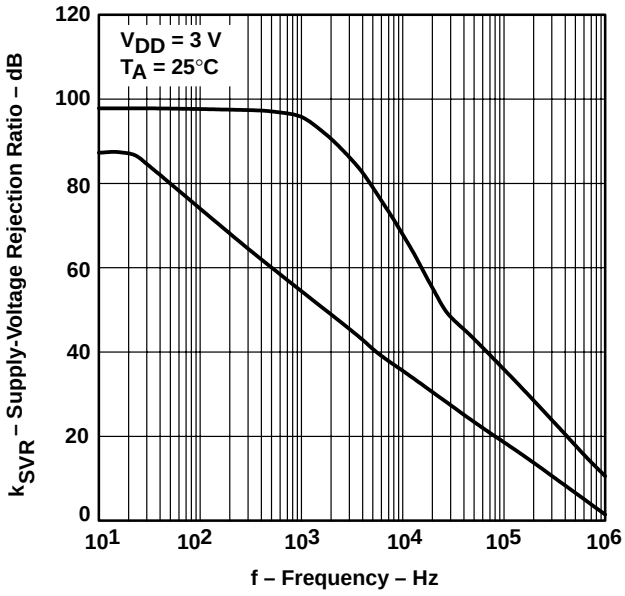


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

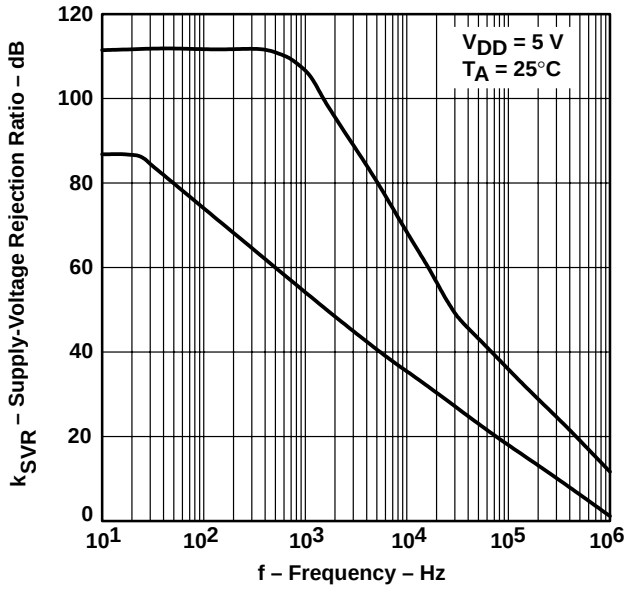


Figure 28

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

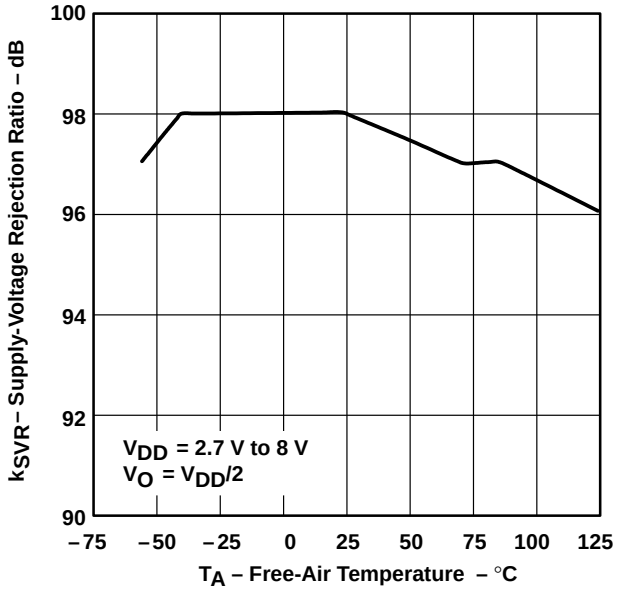


Figure 29

SUPPLY CURRENT vs SUPPLY VOLTAGE

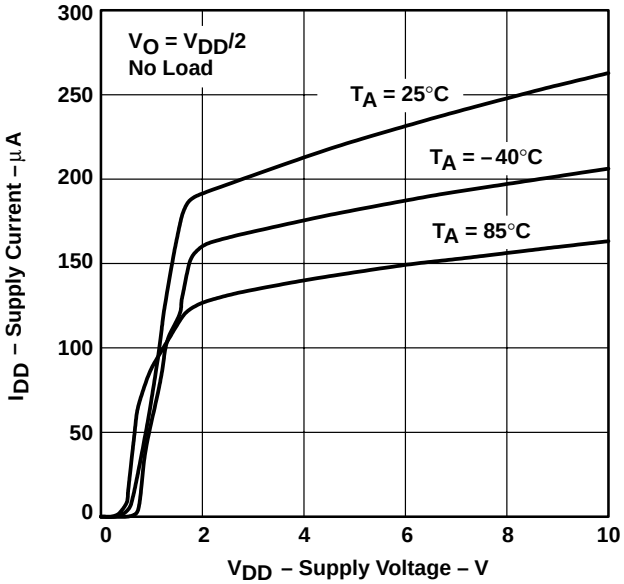


Figure 30

TYPICAL CHARACTERISTICS

SLEW RATE vs LOAD CAPACITANCE

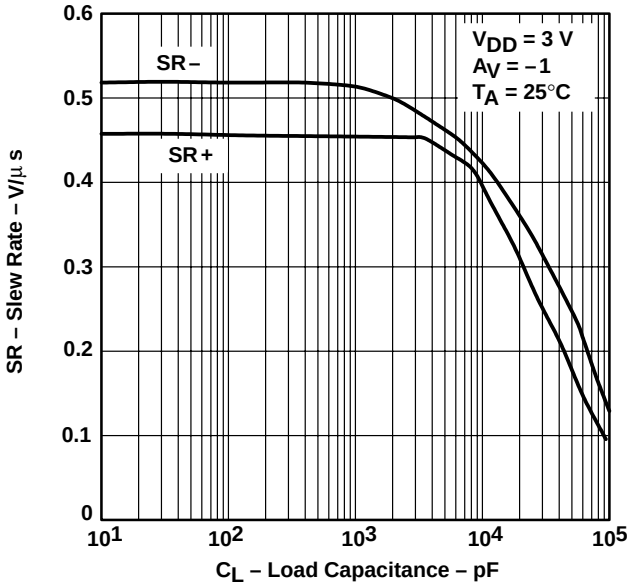


Figure 31

SLEW RATE vs FREE-AIR TEMPERATURE

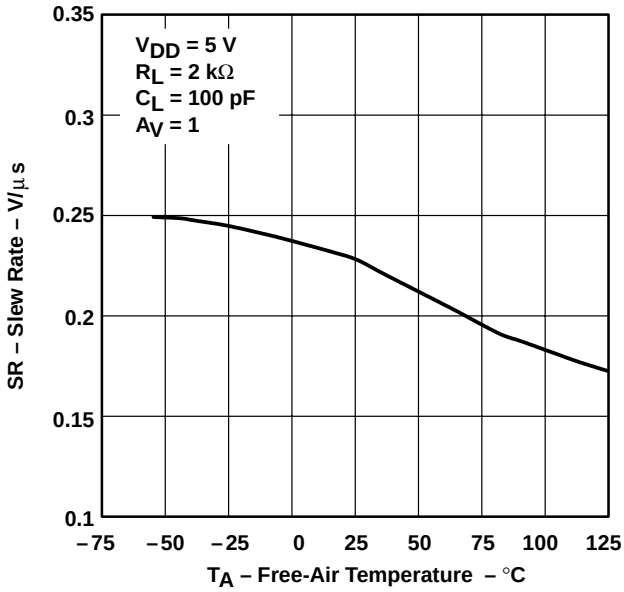


Figure 32

INVERTING LARGE-SIGNAL PULSE RESPONSE

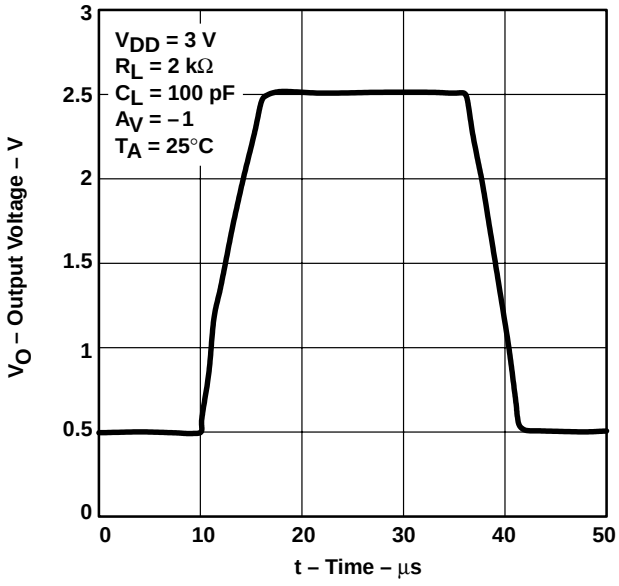


Figure 33

INVERTING LARGE-SIGNAL PULSE RESPONSE

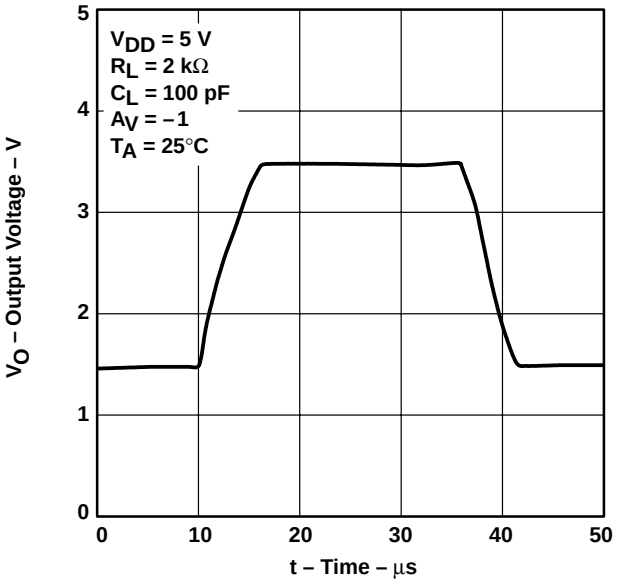


Figure 34

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

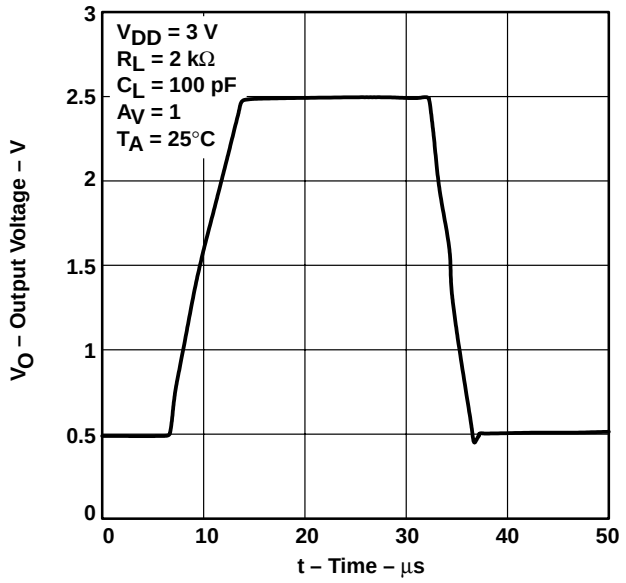


Figure 35

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

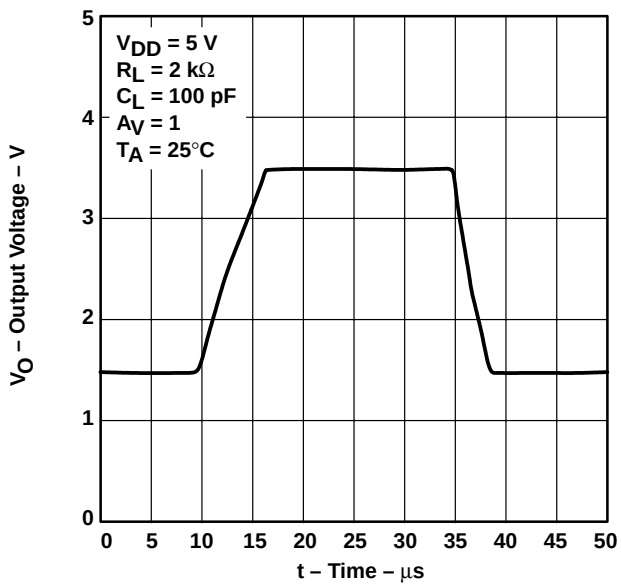


Figure 36

INVERTING SMALL-SIGNAL PULSE RESPONSE

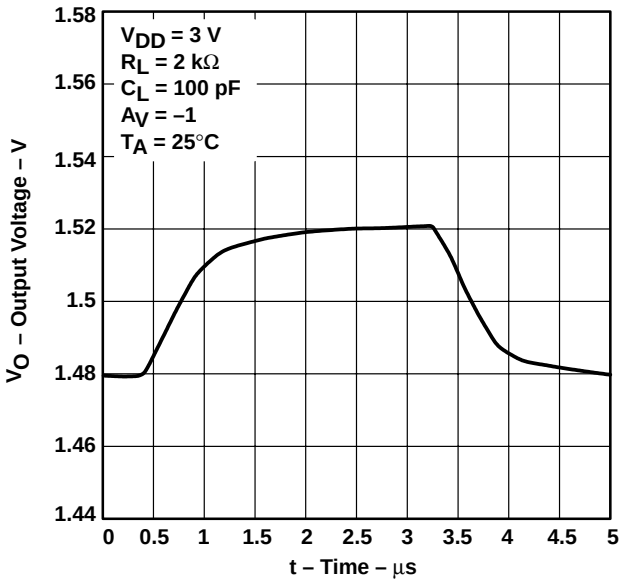


Figure 37

INVERTING SMALL-SIGNAL PULSE RESPONSE

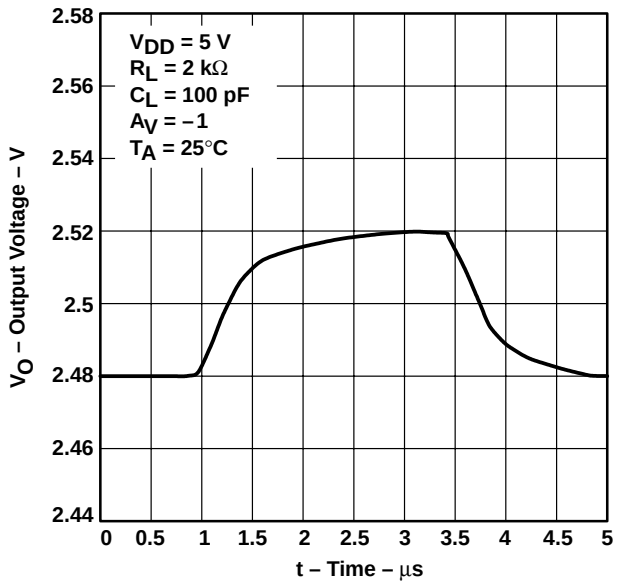


Figure 38

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

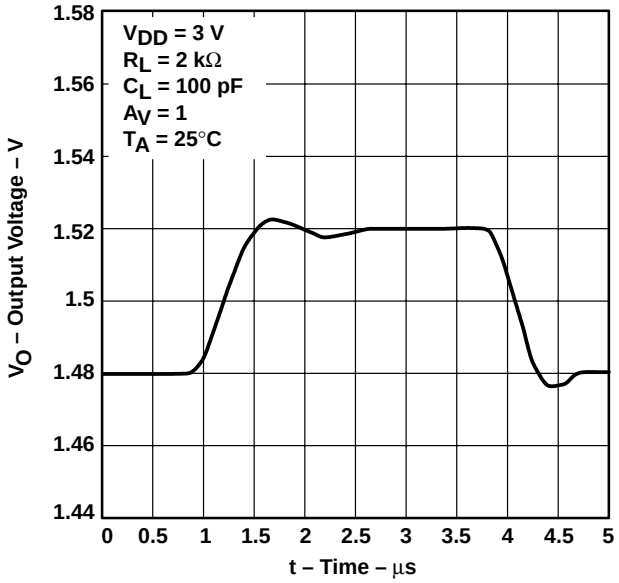


Figure 39

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

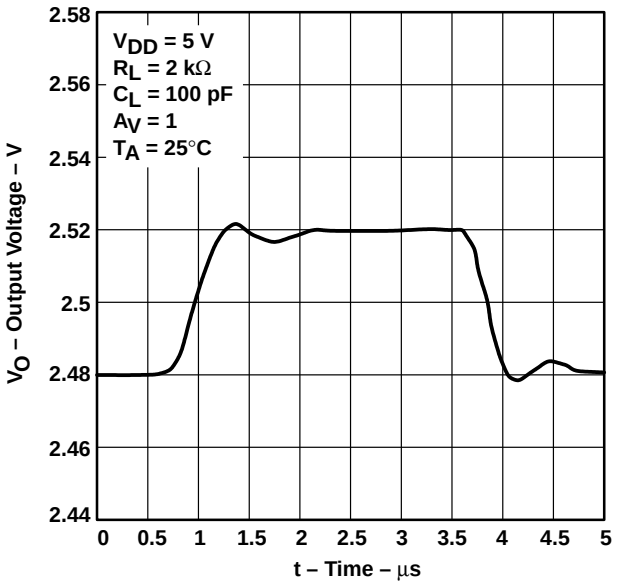


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

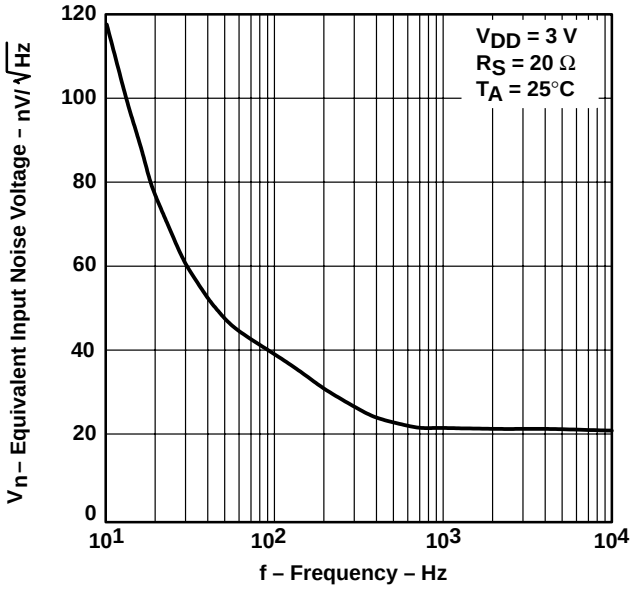


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

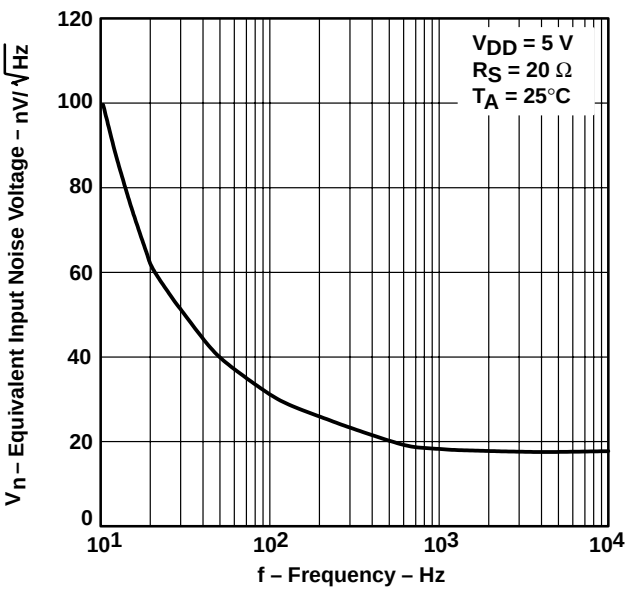


Figure 42

TYPICAL CHARACTERISTICS

NOISE VOLTAGE OVER A 10-SECOND PERIOD

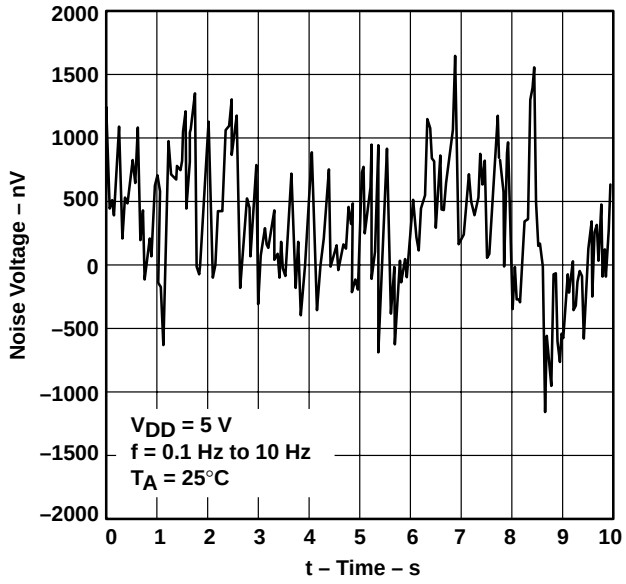


Figure 43

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

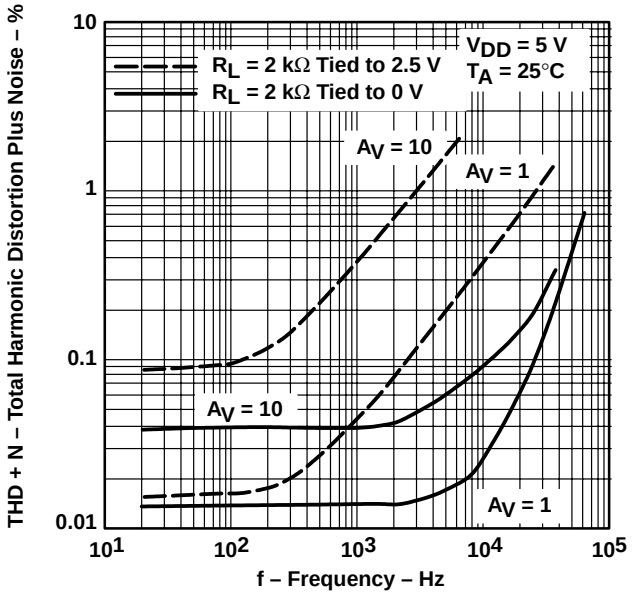


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

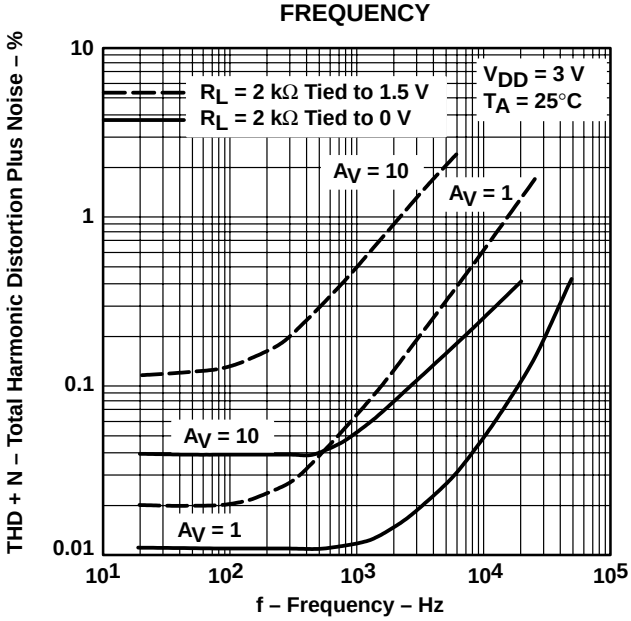


Figure 45

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

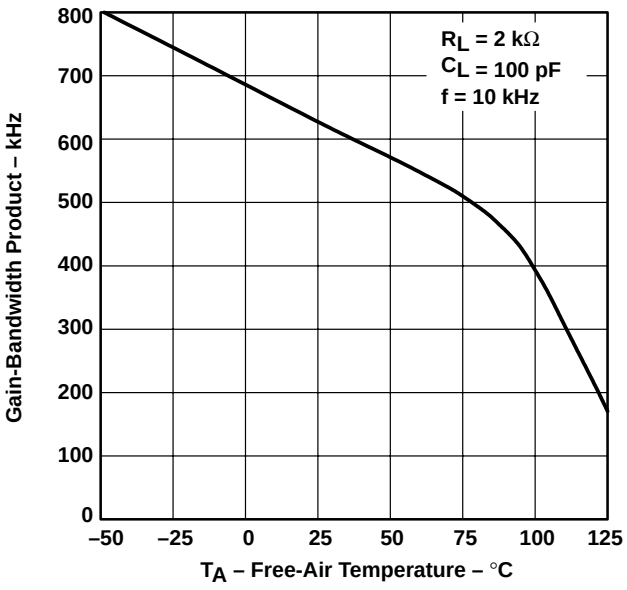


Figure 46

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

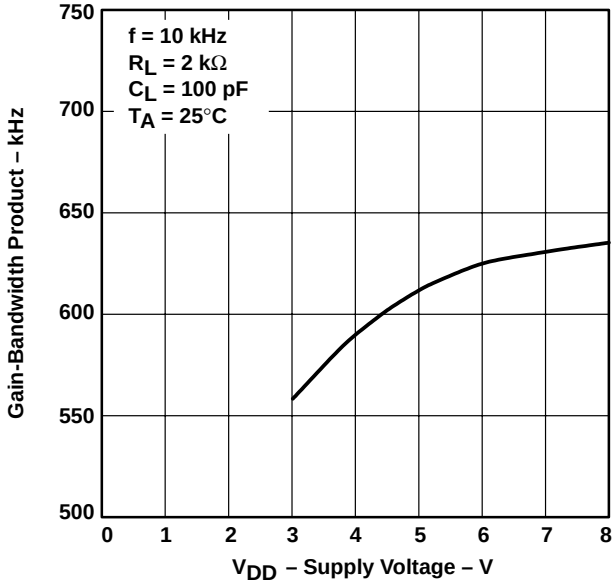


Figure 47

PHASE MARGIN vs LOAD CAPACITANCE

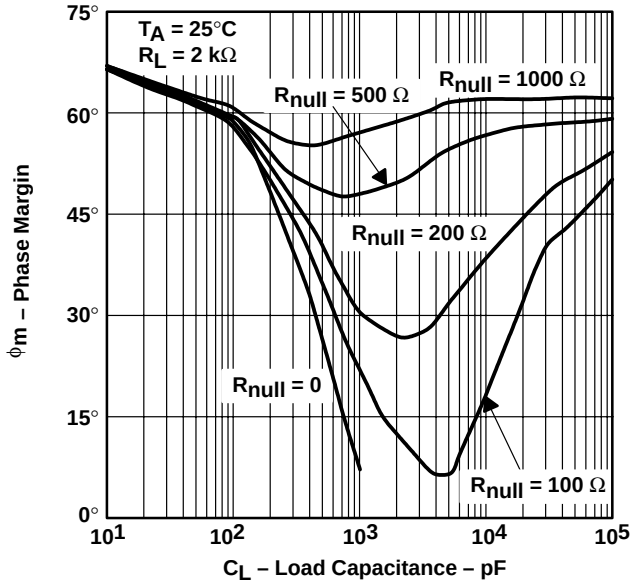


Figure 48

GAIN MARGIN vs LOAD CAPACITANCE

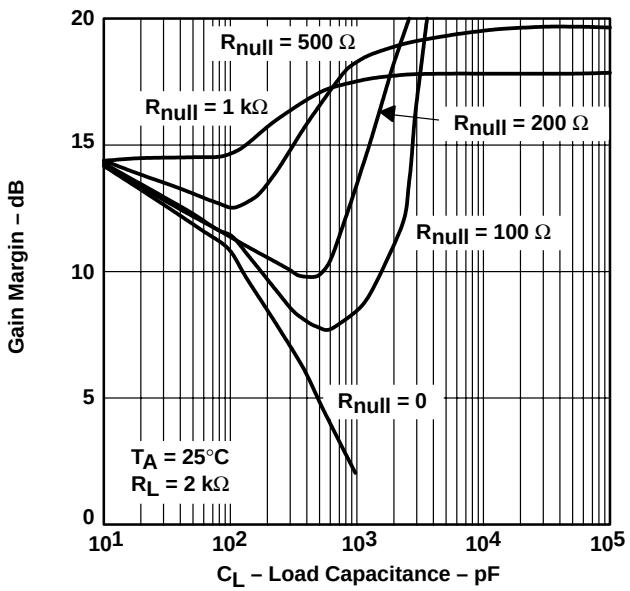


Figure 49

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

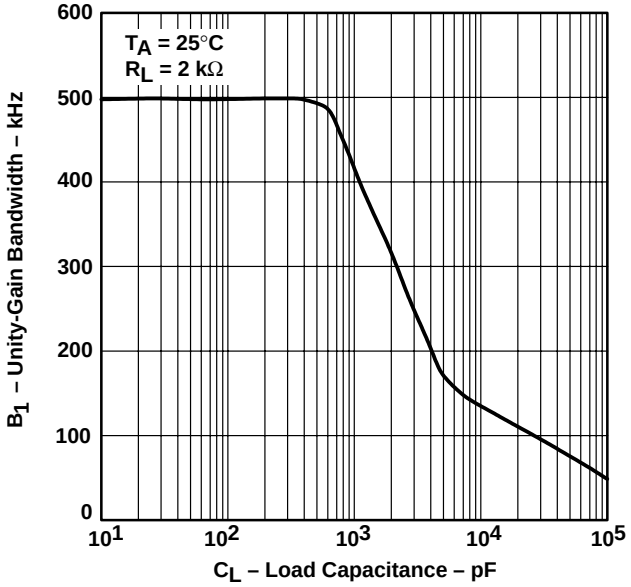


Figure 50

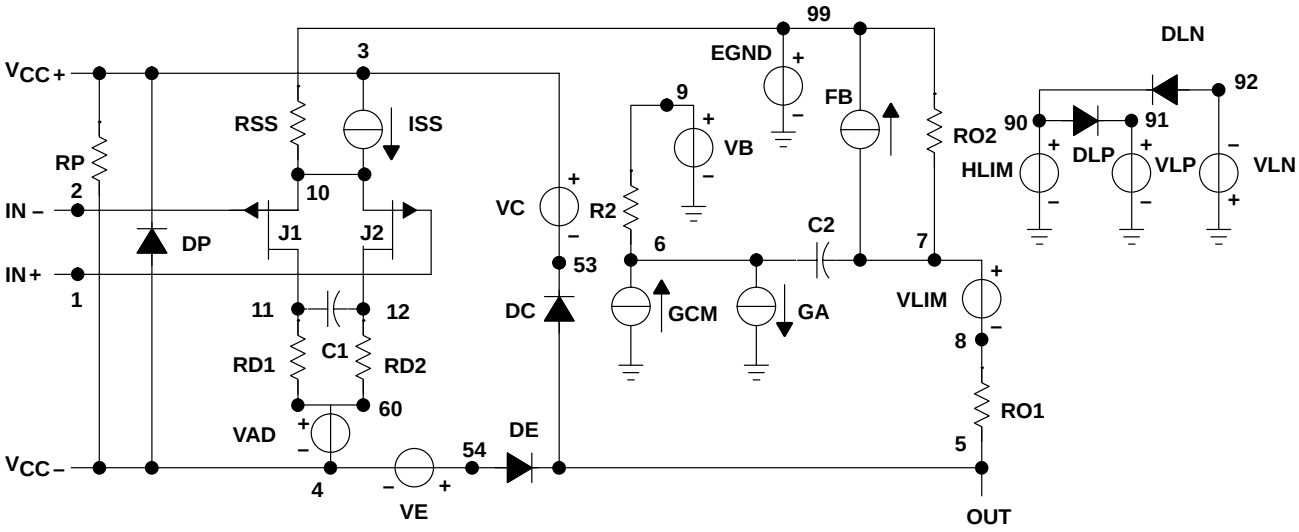
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 51 are generated using the TLV243x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2432 1 2 3 4 5
C1      11    12    3.560E–12
C2      6     7     15.00E–12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 21.04E6 –30E6 30E6 30E6 –30E6
GA      6     0     11    12 47.12E–6
GCM     0     6     10    99 4.9E–9
ISS     3     10    DC 8.250E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    21.22E3
RD2     60    12    21.22E3
R01     8     5     120
R02     7     99    120
RP      3     4     26.04E3
RSS     10    99    24.24E6
VAD     60    4     –.6
VB      9     0     DC 0
VC      3     53    DC .65
VE      54    4     DC .65
VLIM    7     8     DC 0
VLP     91    0     DC 1.4
VLN     0     92    DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=281E–6
+ VTO=–.065)
.ENDS
```

Figure 51. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2432AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2432AI	
TLV2432AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AIPW	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	TV2432	
TLV2432AIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI	Samples
TLV2432AQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A	Samples
TLV2432AQDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A	Samples
TLV2432AQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A	Samples
TLV2432CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	2432C	
TLV2432CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2432C	Samples
TLV2432ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2432I	
TLV2432IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I	Samples
TLV2432QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432Q	Samples
TLV2434AID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	2434AI	
TLV2434AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI	Samples
TLV2434AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI	Samples
TLV2434CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	2434C	
TLV2434CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C	Samples
TLV2434CPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	2434C	
TLV2434CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C	Samples
TLV2434ID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	2434I	
TLV2434IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples
TLV2434IPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	2434I	
TLV2434IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2432, TLV2432A, TLV2434A :

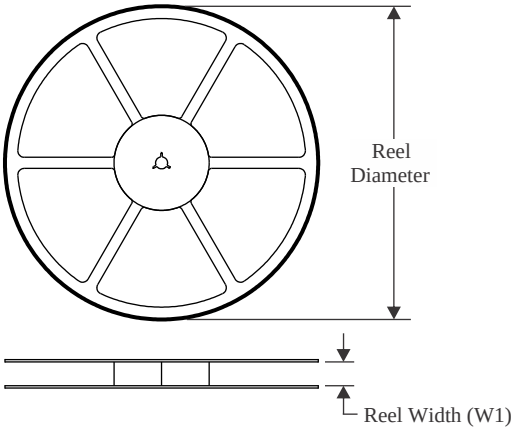
- Automotive : TLV2432-Q1, TLV2432A-Q1, TLV2434A-Q1

NOTE: Qualified Version Definitions:

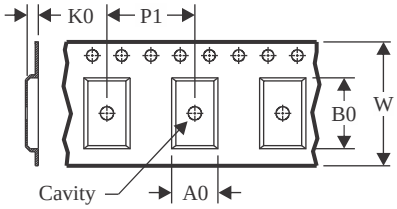
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

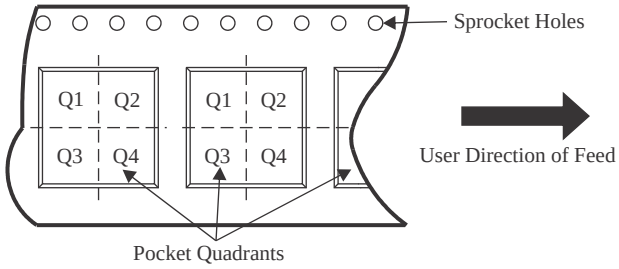


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

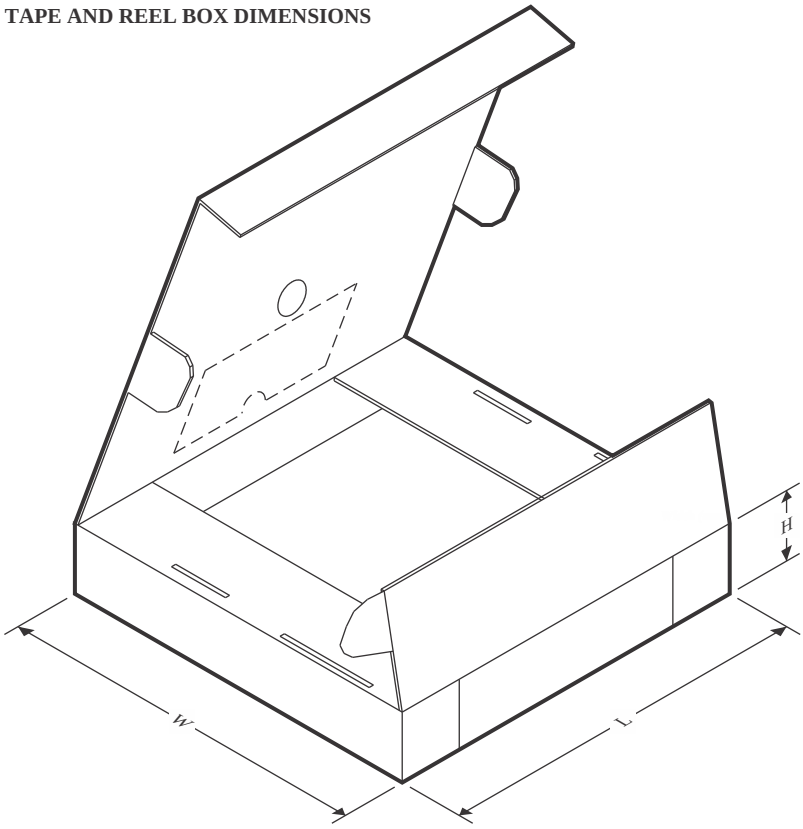
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2432AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2432AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2432CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2434AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

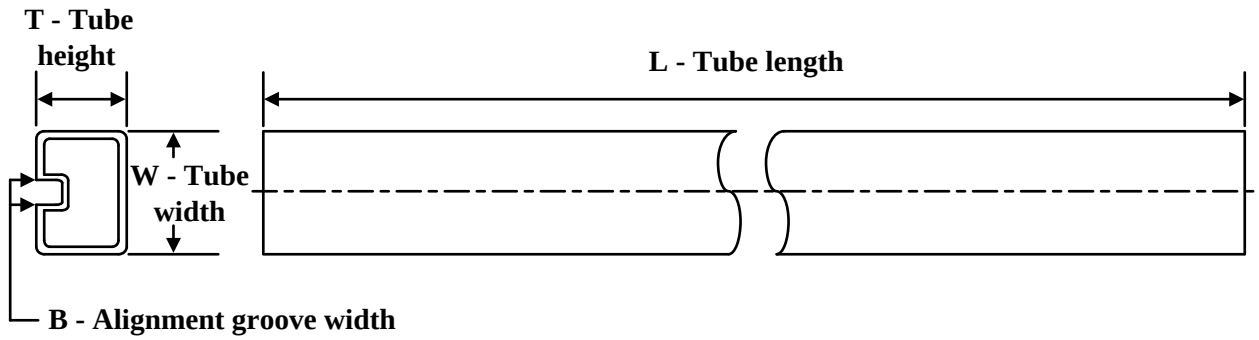
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

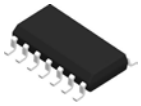
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2432AIDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV2432AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2432AIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2432AIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2432CDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV2432IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2432IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV2434AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2434AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2434AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2434CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2434CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2434CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2434IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV2434IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2434IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2432AQD	D	SOIC	8	75	507	8	3940	4.32
TLV2432AQDG4	D	SOIC	8	75	507	8	3940	4.32
TLV2432QD	D	SOIC	8	75	507	8	3940	4.32

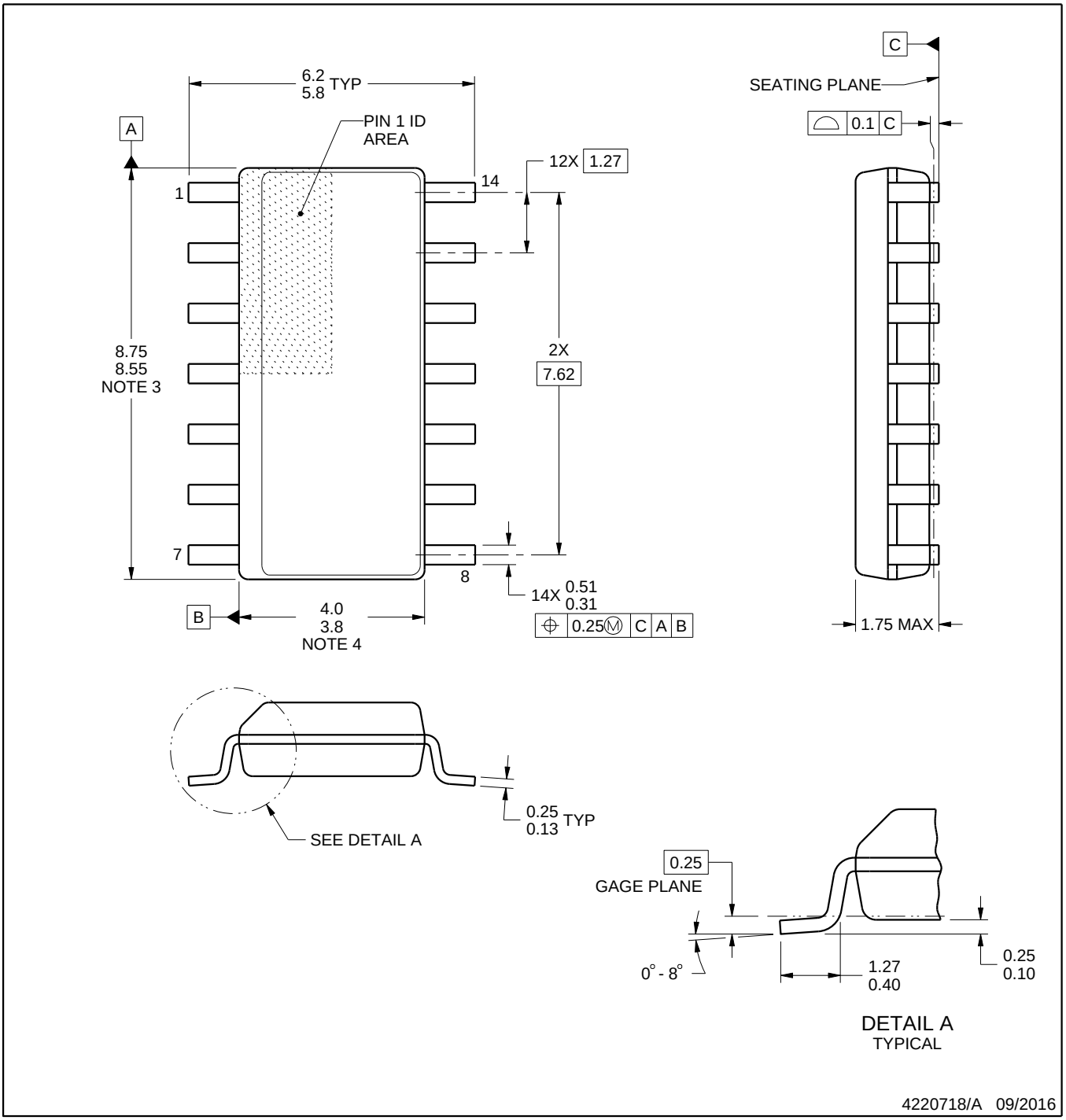


PACKAGE OUTLINE

D0014A

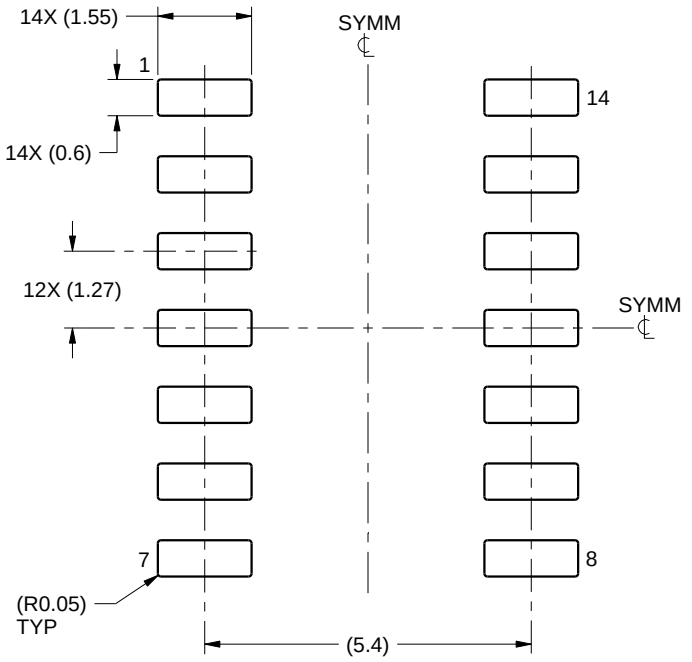
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

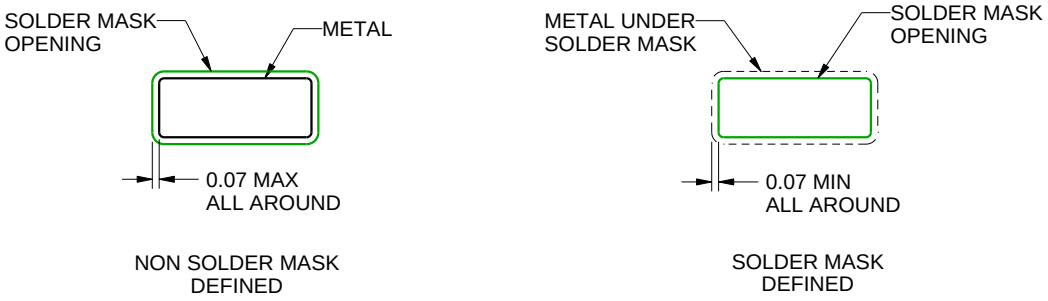


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

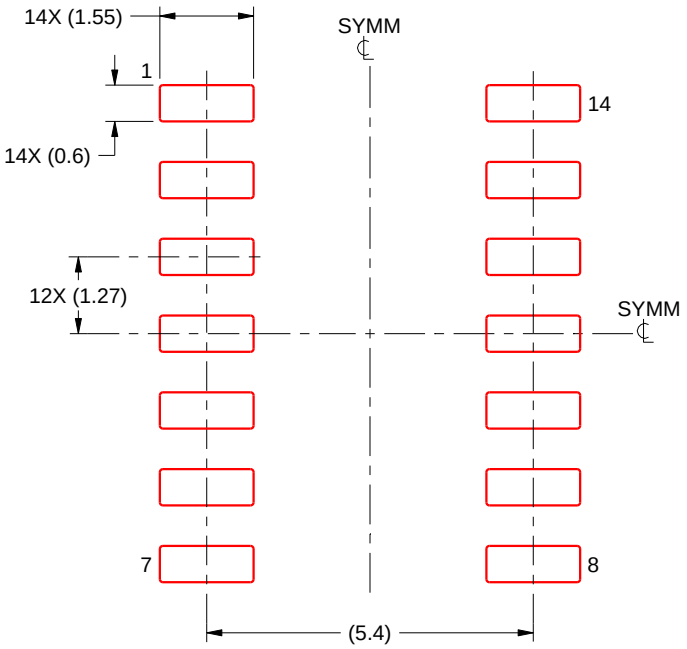
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

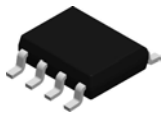


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

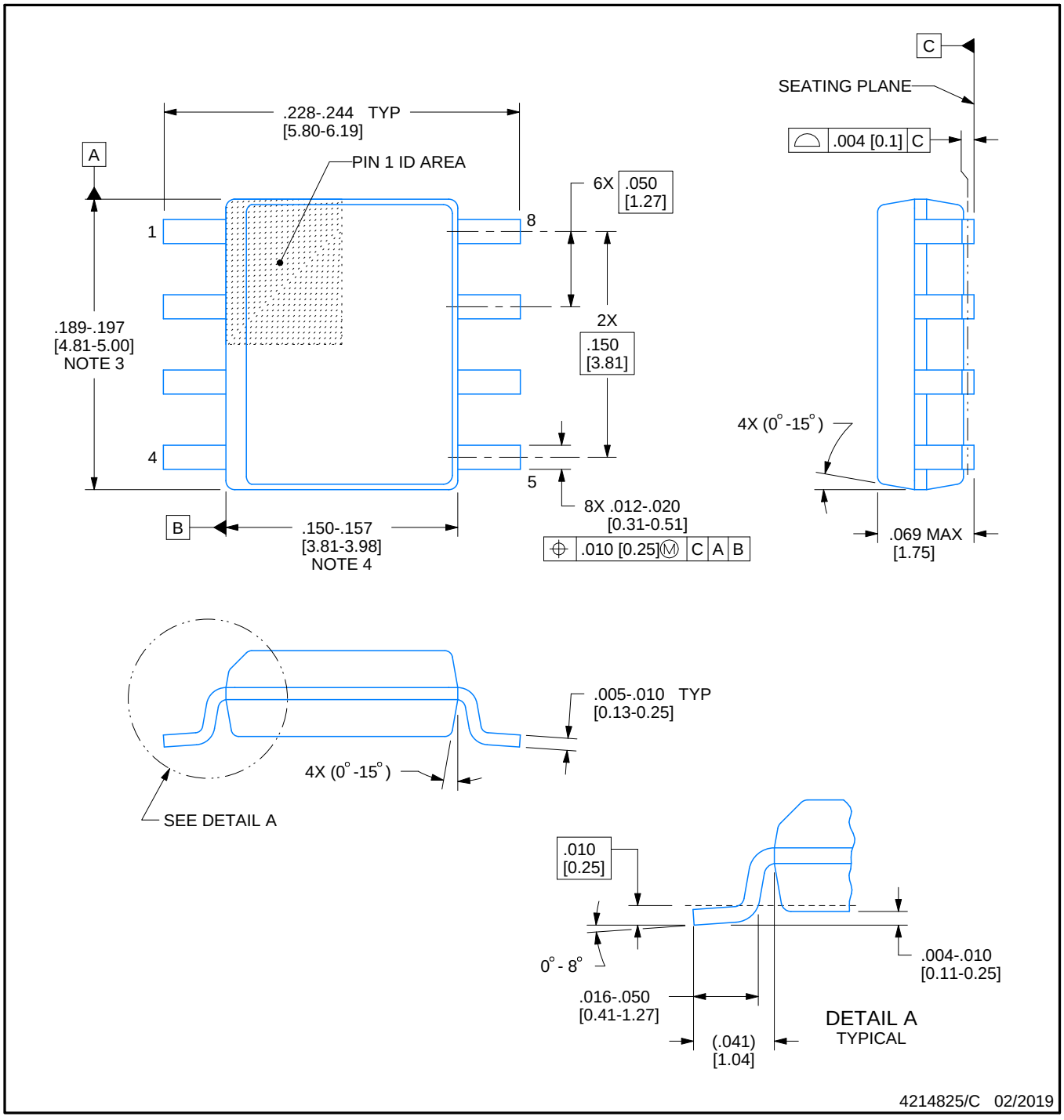


PACKAGE OUTLINE

D0008A

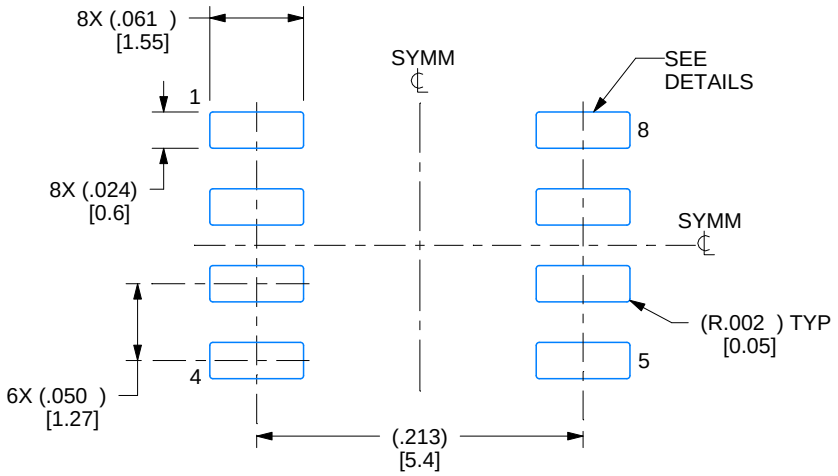
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

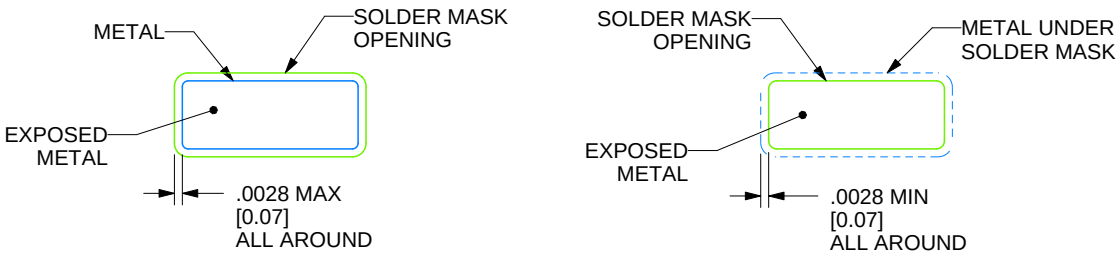


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

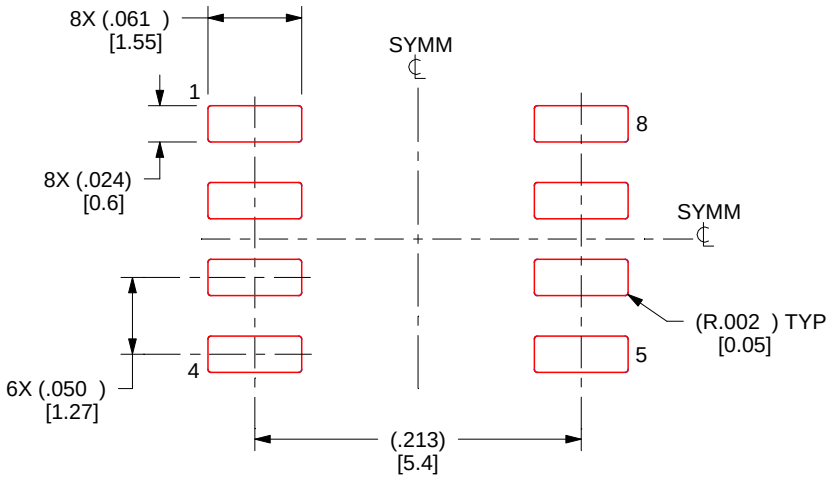
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

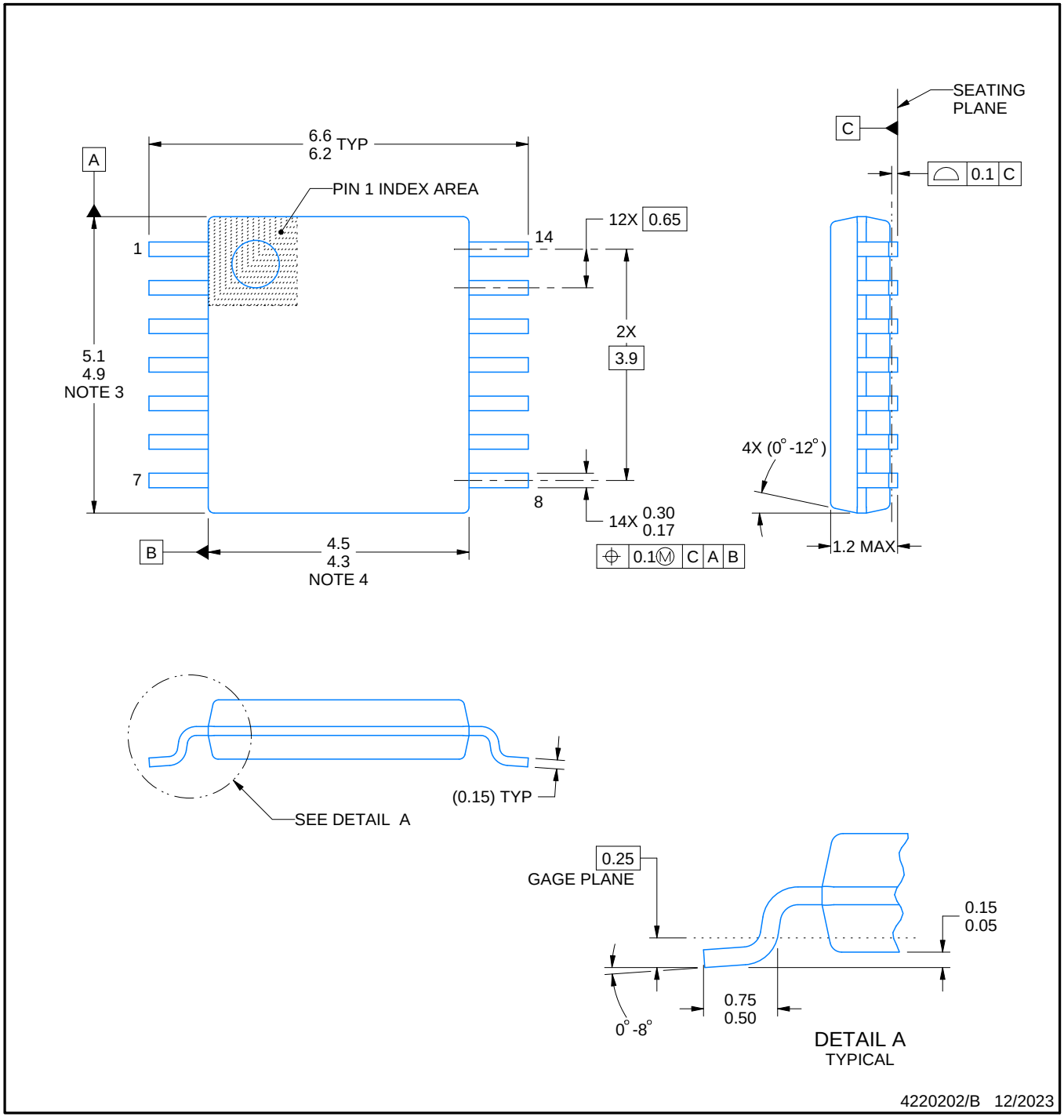
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

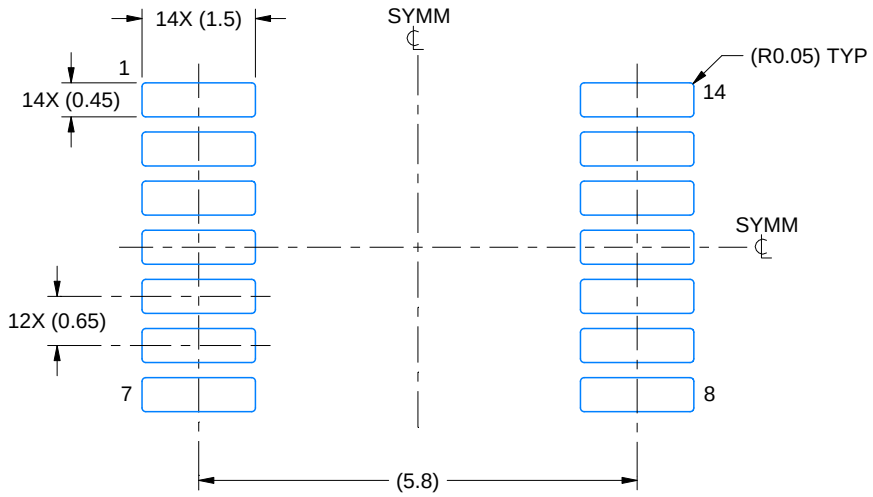
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

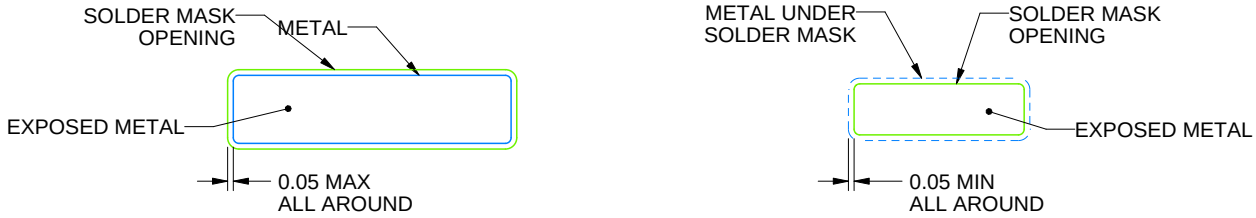


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

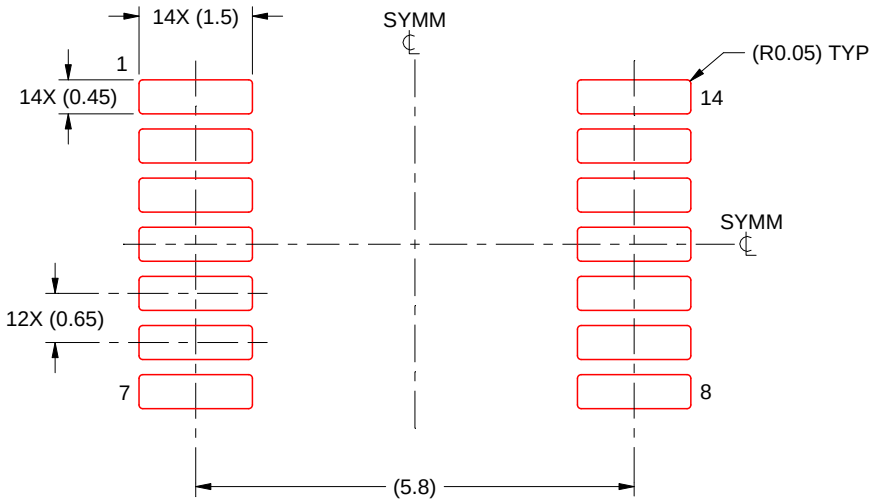


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

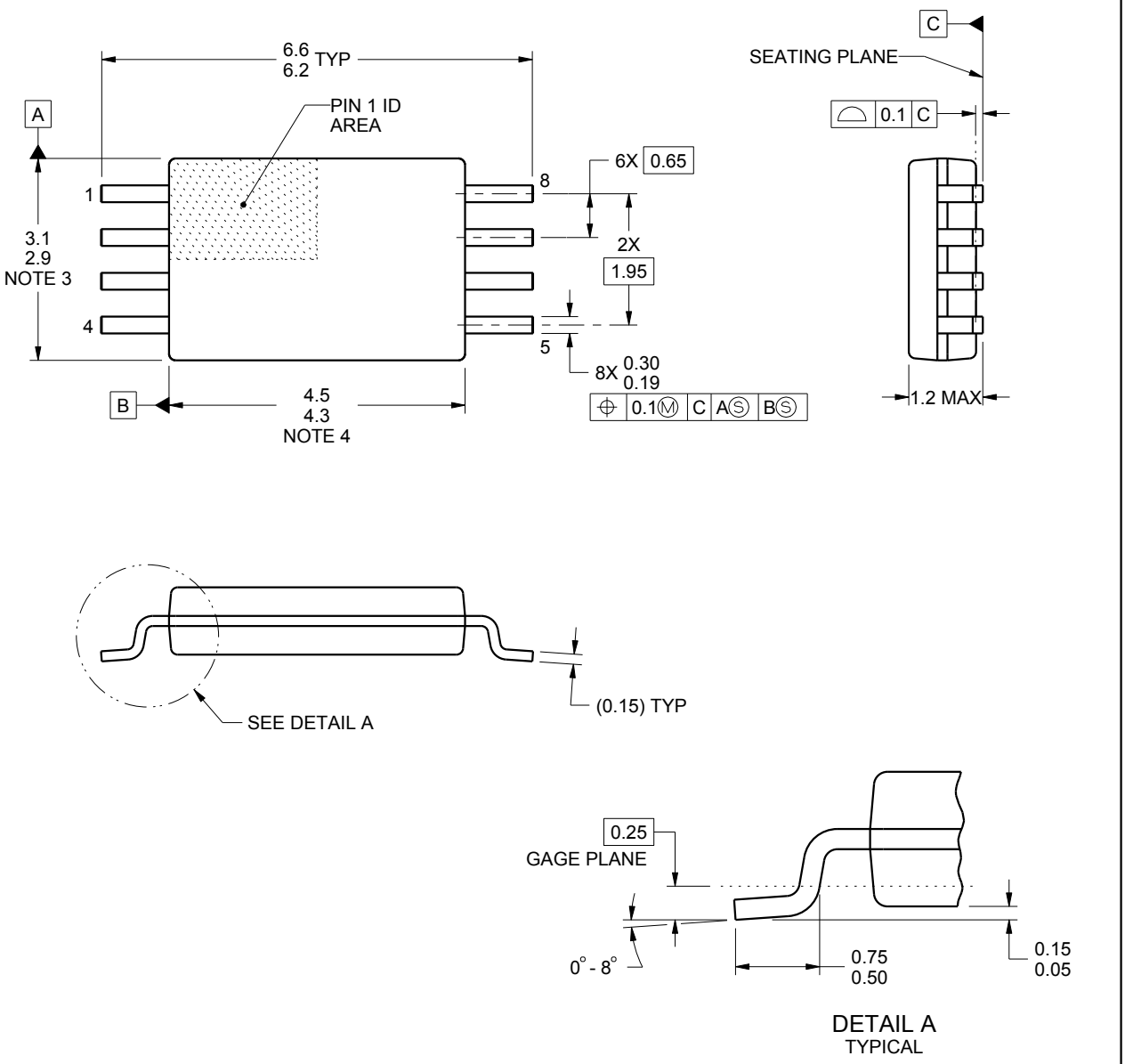
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

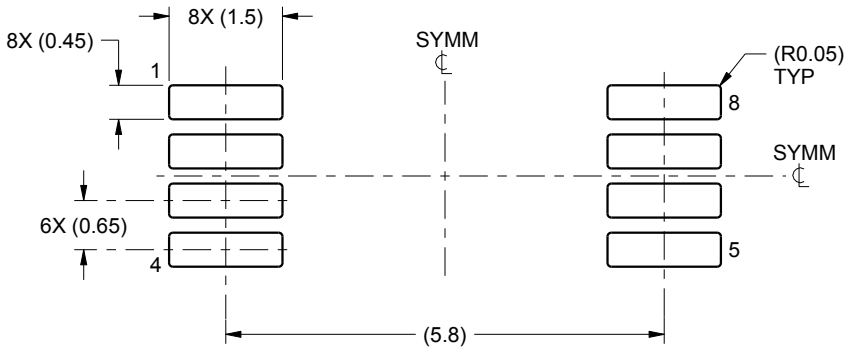
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

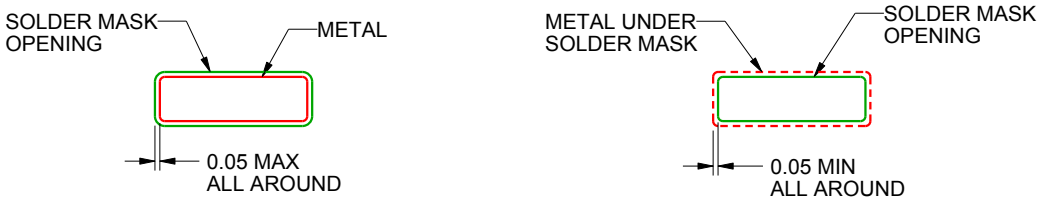


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

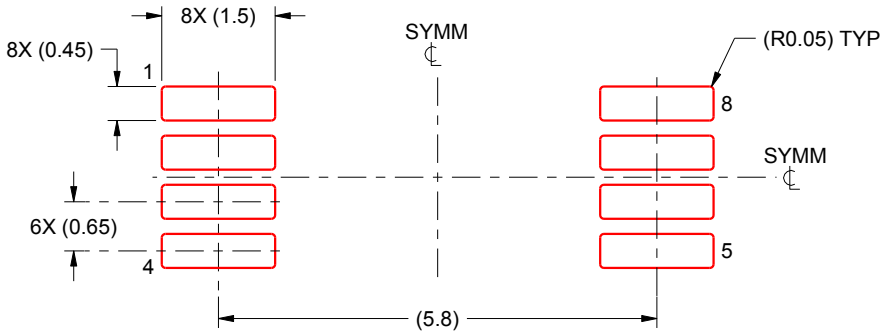


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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